SY88029L

2.5G/10G Dual-Rate Burst Mode Limiting Post Amplifier for XG-PON, XGS-PON, NG-PON2 OLT Transceiver

Features

- Dual-rate Operation 2.5G/10G for XG-PON, XGS-PON, NG-PON2 OLT Receivers
- Optional 1.25G/10G Operation
- Adjustable Decision Threshold Level for BER Optimization
- Wide Differential Input Range: 5 mV_{PP} to 1800 mV_{PP}
- High Sensitivity:
  - 3 mV_{PP} in Continuous Mode
  - 10 mV_{PP} in Burst Mode
- Fast SD Deassert or LOS Assert Times:
  - 110 ns Typical; 150 ns Maximum in AUTORESET Mode
  - 3.5 ns Typical in MANRESET Mode
  - 3.5 dB Typical Electrical Hysteresis
- Selectable LOS or SD Status Signal Indicator
- TTL-Compatible JAM Input with Internal Pull-Up
- Output Polarity Inversion, Crossing, and Output Swing Control
- Low-Noise Swing Programmable CML 10G Outputs with Integrated 45Ω Termination Impedance
  - 30 ps Typical Rise/Fall Times
- Integrated Input Switch for RC Time Constant Control
- Wide Range Power Supply: 3.3V ±10%
- Extended Temperature Range: –40°C to +95°C
- Available in a Small 4 mm x 4 mm QFN Package

Applications

- XG-PON, XGS-PON, NG-PON2
- 10Gigabit Ethernet
- 8 Gbps and 10 Gbps Fibre Channel
- SONET OC192; SDH STM64
- WDM/DWDM Systems

Markets

- PON/FTTx
- Datacom/Enterprise/Telecom
- Storage Area Networks
- High-Performance Computing

General Description

The SY88029L is a dual-rate 2.5G/10G burst mode limiting post amplifier designed for use mainly in XG-PON/XGS-PON and NG-PON2 OLT receivers.

The SY88029L contains a high-sensitivity input stage followed by a 2.5G/10G rate detector/noise discriminator block with user-programmable, wide-range SD assert/LOS deassert threshold levels that enable optimized system reach. Typically, 3.5 dB of electrical hysteresis is provided to minimize LOS or SD chattering caused by noisy input signals, especially if the noise discriminator is disabled. A logic-level control pin is provided to enable user selection of a TTL LOS or SD status indication signal.

The SY88029L provides fast SD assert and LOS deassert times over the entire differential input voltage range of 5 mV_{PP} to 1800 mV_{PP}.
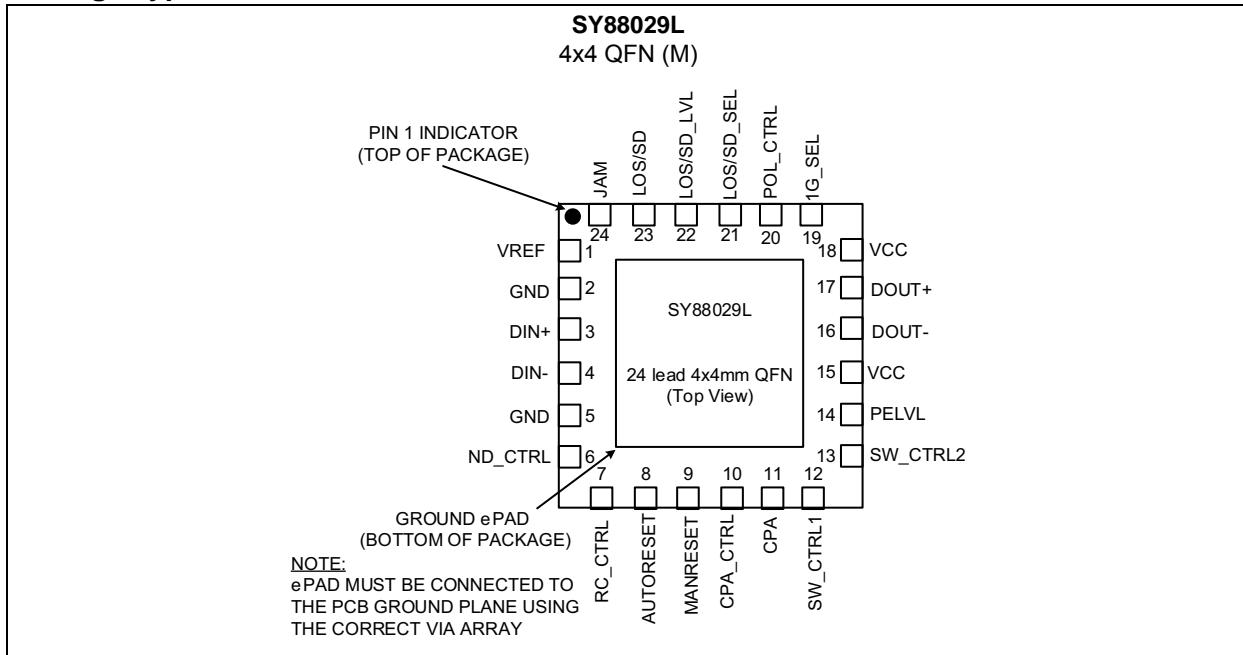
The SY88029L provides a user-adjustable decision threshold circuit to optimize BER in noisy applications. By applying an external control voltage, the decision threshold can typically be adjusted from 35% to 75% from the nominal 50% threshold when the circuit is disabled.

The SY88029L provides an integrated 20 kΩ input termination and a switch to add a 10Ω parallel to it for RC time constant control. The CML output has a 45Ω internal termination. The post amplifier features output swing control, pre-emphasis, and polarity inversion to simplify PCB layout. A TTL-compatible JAM input is provided to enable a SQUELCH function by feeding back the LOS or SD signal. The JAM input disables only the post amplifier output.
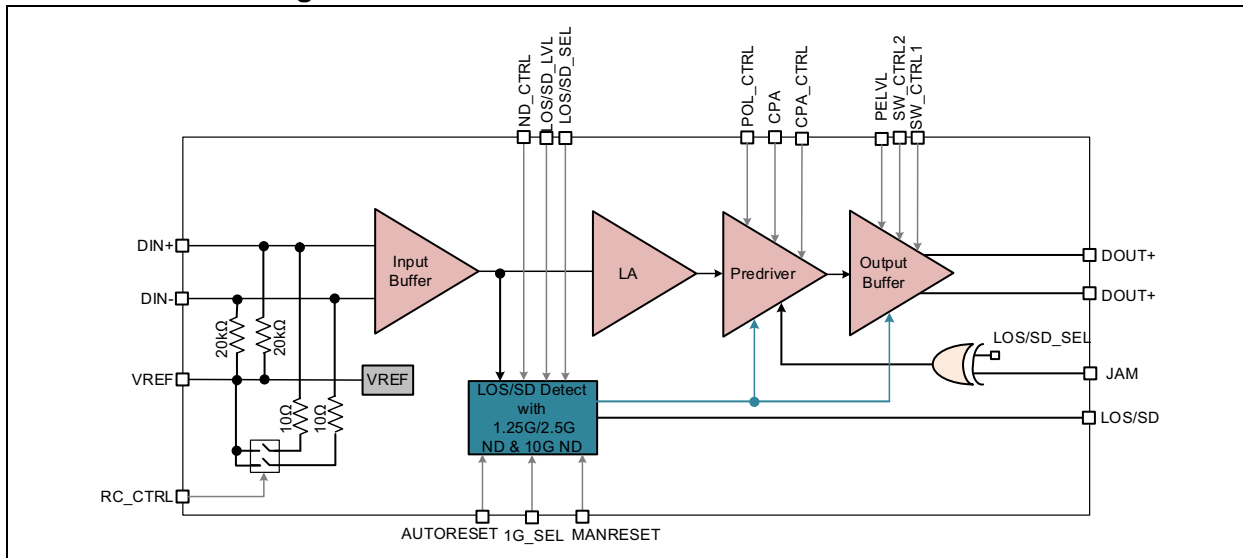
The SY88029L operates from a single +3.3V power supply, over temperatures ranging from –40°C to +95°C.

SY88029L

Package Type

SY88029L
4x4 QFN (M)

SY88029L
24 lead 4x4mm QFN
(Top View)

PIN 1 INDICATOR
(TOP OF PACKAGE)

Pin	Signal
24	JAM
23	LOS/SD
22	LOS/SD_LVL
21	LOS/SD_SEL
20	POL_CTRL
19	1G_SEL

Pin	Signal
1	VREF
2	GND
3	DIN+
4	DIN-
5	GND
6	ND_CTRL

Pin	Signal
18	VCC
17	DOUT+
16	DOUT-
15	VCC
14	PELVL
13	SW_CTRL2

Pin	Signal
7	RC_CTRL
8	AUTORESET
9	MANRESET
10	CPA_CTRL
11	CPA
12	SW_CTRL1

GROUND ePAD
(BOTTOM OF PACKAGE)

NOTE:
ePAD MUST BE CONNECTED TO
THE PCB GROUND PLANE USING
THE CORRECT VIA ARRAY

Functional Block Diagram

SY88029L

TABLE 1-1:   ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{CC} = 3.0 to 3.6V; T_A = –40°C to +95°C. Typical values at V_{CC} = 3.3V, T_A = +25°C unless otherwise indicated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
Power Supply Current	I_{CC}	—	98	123	mA	ND_CTRL Low
		—	112	139		ND_CTRL High
Additional Pre-Emphasis Current	I_{PE}	—	10	12	mA	PE ON
DC Signals						
LOS/SD_LVL Voltage	LOS/SD_LVL	V_{CC} – 1.0V	—	V_{CC} – 0.6V	V	—
Reference Voltage for Input Terminations	V_{REF}	—	V_{CC} – 1.25	—	V	90 µA maximum current source/sink
Pre-Emphasis Level Setting Input Voltage	PELVL	0	1.25	2.5	V	—
Cross Point Adjust Setting Input Voltage	CPA	0	1.25	2.5	V	—
LVTTL Signals						
LVTTL Input HIGH Voltage	V_{IH}	2.0	—	—	V	JAM, LOS/SD_SEL, POL_CTRL, SW_CTRL1, SW_CTRL2, CPA_CTRL, MANRESET, AUTORESET, ND_CTRL, RC_CTRL, 1G_SEL
LVTTL Input LOW Voltage	V_{IL}	—	—	0.8	V	
LOS/SD Output HIGH Level	V_{OH}	2.4	—	—	V	—
LOS/SD Output LOW Level	V_{OL}	—	—	0.5	V	—
CML Output						
Differential Output Voltage Swing	V_{OD}	—	—	—	mV$_{PP}$	$V_{ID} \geq$ 18mVPP Note 1
						SW_CTRL1 SW_CTRL2
		—	380	—		LOW LOW
		—	560	—		LOW HIGH
		—	750	—		HIGH LOW
		—	850	—		HIGH HIGH

Note 1: V_{OD} is measured with 50Ω load to V_{CC}.

    2: Amplifier in limiting mode. Input is a 200 MHz square wave.

    3: Measured using K28.5 pattern, V_{ID} = 10 mV$_{PP}$.

    4: Measured using K28.7 pattern, V_{ID} = 10 mV$_{PP}$.

    5: SD is the opposite polarity of LOS. Therefore, an SD assert parameter is equivalent to a LOS deassert parameter and vice versa.

    6: This specification defines electrical hysteresis as 20log(SD assert/SD deassert).

    7: All SD assert (LOS deassert) level, SD deassert (LOS assert) level, and hysteresis specifications listed above are specified using a 1010 pattern.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{CC} = 3.0 to 3.6V; T_A = –40°C to +95°C. Typical values at V_{CC} = 3.3V, T_A = +25°C unless otherwise indicated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Differential Output DC Voltage Swing	V_{ODOFF}	—	100	120	mV_{PP}	Output powered down (ND_CTRL = High, Detection Mode)
Differential Output Offset	V_{OFFSET}	—	—	±80	mV	CPA not used, V_{ID} = 0V, SW_CTRL1 = High, SW_CTRL2 = High
Output Rise/Fall Time (20% to 80%)	t_r/t_f	—	30	35	ps	Note 2
Deterministic Jitter	t_{JITTER}	—	3	—	ps_{PP}	Note 3
Random Jitter	—	—	1	—	ps_{RMS}	Note 4
Single Ended Output Impedance	Z_O	40	45	50	Ω	—
Differential Voltage Gain	$A_{V(DIFF)}$	—	46	—	dB	—
Single-Ended Small-Signal Gain	S_{21}	—	40	—	dB	—
DIN Input						
Differential Input Voltage Swing	V_{ID}	5	—	1800	mV_{PP}	—
Single-Ended Input Impedance	Z_I	—	20	—	kΩ	Switch open, RC_CTRL Low
		—	10	—	Ω	Switch closed, RC_CTRL High
LOS/SD						
JAM Enable/Disable Time	t_{JAM}	—	—	2	ns	—
SD Deassert or LOS Assert with Auto Reset Enabled	$t_{AUTORESET}$	75	110	150	ns	—
MANRESET Pulse Width	$t_{MANRESET}$	5	—	—	ns	—
SD Deassert or LOS Assert with MANRESET	t_{RESET}	—	—	5	ns	—
SD Assert Time/LOS Deassert Time	t_{ON}	—	—	5	ns	Noise Discriminator Disabled, 15 pF load

Note 1: V_{OD} is measured with 50Ω load to V_{CC}.
2: Amplifier in limiting mode. Input is a 200 MHz square wave.
3: Measured using K28.5 pattern, V_{ID} = 10 mV_{PP}.
4: Measured using K28.7 pattern, V_{ID} = 10 mV_{PP}.
5: SD is the opposite polarity of LOS. Therefore, an SD assert parameter is equivalent to a LOS deassert parameter and vice versa.
6: This specification defines electrical hysteresis as 20log(SD assert/SD deassert).
7: All SD assert (LOS deassert) level, SD deassert (LOS assert) level, and hysteresis specifications listed above are specified using a 1010 pattern.

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TABLE 1-1:   ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{CC} = 3.0 to 3.6V; T_A = –40°C to +95°C. Typical values at V_{CC} = 3.3V, T_A = +25°C unless otherwise indicated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
SD Assert Time/LOS Deassert Time	t_{ON_ND}	—	—	7 (10G)	ns	Noise Discriminator Enabled, 15 pF load
		—	—	15 (2.5G)		
SD Deassert/LOS Assert Level	LOS_{A_10k}	—	3.3	—	mV_{PP}	R_{LOSLVL} = 10 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 1.0V
SD Assert/LOS Deassert Level	LOS_{D_10k}	—	4.7	—	mV_{PP}	R_{LOSLVL} = 10 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 1.0V
LOS/SD Hysteresis	HYS_{10k}	2	3.1	6	dB	R_{LOSLVL} = 10 kΩ, Note 6 LOS/SD_LVL = V_{CC} − 1.0V
SD Deassert/LOS Assert Level	LOS_{A_5k}	—	4.0	—	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 0.8V
SD Assert/LOS Deassert Level	LOS_{D_5k}	—	5.8	—	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 0.8V
LOS/SD Hysteresis	HYS_{5k}	2	3.2	6	dB	R_{LOSLVL} = 5 kΩ, Note 6 LOS/SD_LVL = V_{CC} − 0.8V
SD Deassert/LOS Assert Level	$LOS_{A\_2.5k}$	—	5.3	—	mV_{PP}	R_{LOSLVL} = 2.5 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 0.6V
SD Assert/LOS Deassert Level	$LOS_{D\_2.5k}$	—	7.9	—	mVPP	R_{LOSLVL} = 2.5 kΩ, Note 5, Note 7 LOS/SD_LVL = V_{CC} − 0.6V
LOS/SD Hysteresis	$HYS_{2.5k}$	2	3.6	6	dB	R_{LOSLVL} = 2.5 kΩ, Note 6 LOS/SD_LVL = V_{CC} − 0.6V

Note 1: V_{OD} is measured with 50Ω load to V_{CC}.

   2: Amplifier in limiting mode. Input is a 200 MHz square wave.

   3: Measured using K28.5 pattern, V_{ID} = 10 mV_{PP}.

   4: Measured using K28.7 pattern, V_{ID} = 10 mV_{PP}.

   5: SD is the opposite polarity of LOS. Therefore, an SD assert parameter is equivalent to a LOS deassert parameter and vice versa.

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   7: All SD assert (LOS deassert) level, SD deassert (LOS assert) level, and hysteresis specifications listed above are specified using a 1010 pattern.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+95	°C	—
Junction Operating Temperature	T_J	—	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 20 sec.
Package Thermal Resistances (Note 2)						
Thermal Resistance, 4x4 QFN-16LD	θ_{JA}	—	61	—	°C/W	Still-Air
Thermal Resistance, 4x4 QFN-16LD	Ψ_{JB}	—	30.5	—	°C/W	Junction-to-Board

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e. T_A, T_J, Ψ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperature above +125°C can impact the device reliability.

2: Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

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2.0   TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.
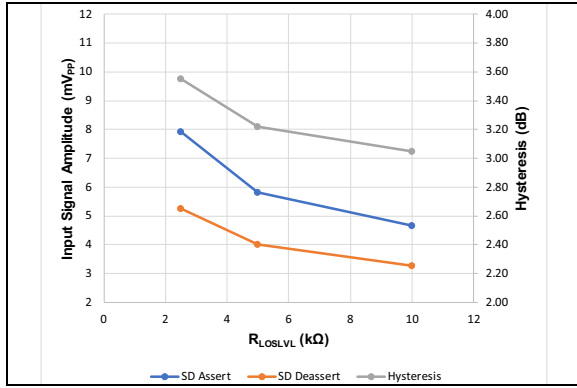
FIGURE 2-1:   *SD Assert/Deassert and Hysteresis vs. R_{LOSLVL} with Continuous Mode Input Signal.*

FIGURE 2-2:   *10G Eye Diagram (V_{IN} = 20 mV_{PP}).*

FIGURE 2-3:   *10G Eye Diagram (V_{IN} = 5 mV_{PP}).*

FIGURE 2-4:   *10G Eye Diagram with CPA Enabled (CPA_CTRL = High), CPA = 0V.*

FIGURE 2-5:   *10G Eye Diagram with CPA Enabled (CPA_CTRL = High), CPA = 1.6V.*
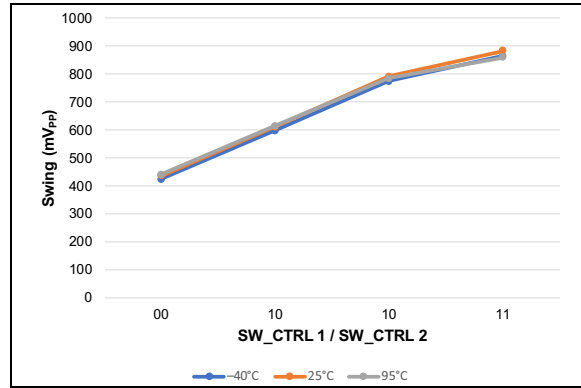
FIGURE 2-6:   *CML Output Swing vs. Temperature (V_{CC} = 3.3V).*

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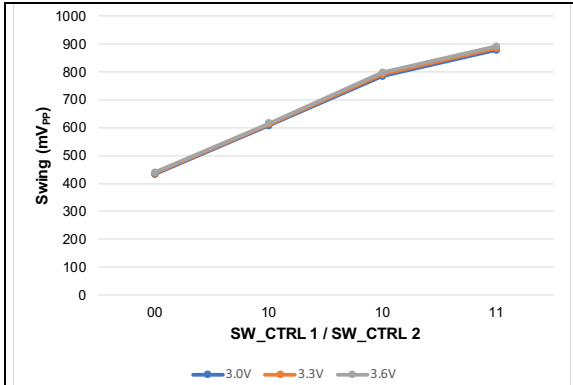
FIGURE 2-7: *CML Output Swing vs. V_{CC} (T = +25°C).*
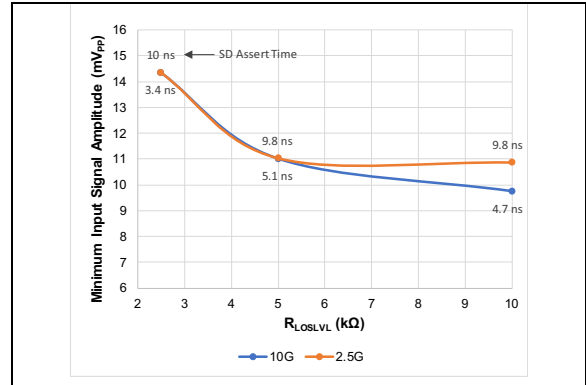
FIGURE 2-9: *Typical Burst Mode Sensitivity.*
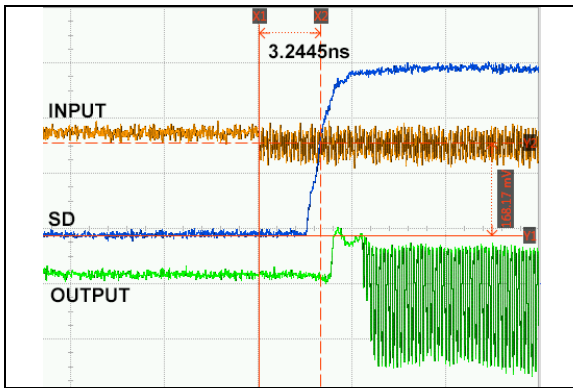
FIGURE 2-8: *10G Burst Detection Time with R_{LOSLVL} = 10 kΩ.*
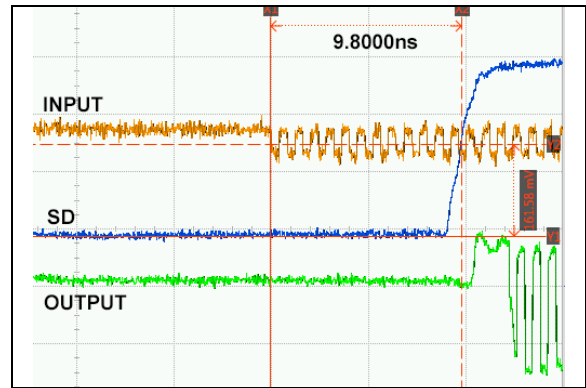
FIGURE 2-10: *2.5G Burst Detection Time with R_{LOSLVL} = 10 kΩ.*

SY88029L

3.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1:   PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VREF	Reference Voltage Output. Typically V_{CC} – 1.25V. Limited source/sink capabilities. To be used for input termination/biasing only.
2, 5	GND	Negative Supply Rail. Connect to the PCB negative power supply plane that is also connected to the ePAD.
3	DIN+	Data Inputs. Internally terminated to VREF with 20 kΩ. AC-coupled only. SY88029L has an internal switch that allows to short the 20 kΩ resistor with a 10Ω resistor.
4	DIN–	
6	ND_CTRL	Noise Discriminator Control. LVTTL input with internal 25 kΩ pull-up resistor. Connect to VCC, keep floating, or apply a high LVTTL signal to enable ND. Connect to GND or apply a low LVTTL signal to disable ND.
7	RC_CTRL	Input RC Time Constant Control. LVTTL input with 25 kΩ pull-down. Leave open or apply low level to open the internal switch and use 20 kΩ to get a long RC time constant. Apply a high level to close the switch and short the 20 kΩ with a low resistor to get a short RC time constant.
8	AUTORESET	Automatic RESET. LVTTL Input. This pin is internally connected to a 25 kΩ pull-up resistor and defaults to HIGH. When this pin is left floating or a high LVTTL signal is applied, the AUTORESET function is enabled and SD deasserts or LOS asserts within 110 ns (typical) after the last transition of the burst input. When this pin is LOW or tied to ground, the AUTORESET function is disabled and the SD deassert or LOS assert must be forced by using the manual reset function (MANRESET).
9	MANRESET	Manual RESET. LVTTL Input. Apply a high-level signal to this pin for 5 ns to reset the LOS/SD signal within fewer than 5 ns. If the AUTORESET function is not used, this manual RESET function needs to be used to deassert the SD or assert LOS. This pin is internally connected to a 25 kΩ pull-down resistor and defaults to LOW.
10	CPA_CTRL	Input Crossing Point Adjust Control. LVTTL input with internal 25 kΩ pull-down resistor to GND. Leave open or apply low TTL to disable the crossing point adjust function. Connect to VCC or apply a high TTL signal to enable CPA function. Apply a DC voltage at the CPA pin to control the eye crossing.
11	CPA	Crossing Point Adjust Positive Side. To use crossing control, apply a high level to the CPA_CTRL pin and apply a DC voltage from 0V to 2.5V on the CPA pin to adjust signal crossing. The internal reference (negative side) is at 1.25V.
12	SW_CTRL1	Output Swing Control. LVTTL inputs. Allows the user to select between different amplitudes of DOUT+/-. See Table 1-1 for details. These pins are internally connected to 25 kΩ pull-down resistors and default to LOW.
13	SW_CTRL2	
14	PELVL	Pre-Emphasis Level. Apply a voltage within the range of 0V – 2.5V to set the pre-emphasis to be applied to the output signal. 0V provides maximum pre-emphasis and 2.5V provides minimum pre-emphasis. Connect to VCC to turn off PE.
15, 18	VCC	Positive power supply input. Bypass with a 0.1 µF capacitor in parallel with a 0.01 µF low-ESR capacitor to GND as close as possible to the VCC pins.
16	DOUT–	CML Outputs. When JAM disables the device, output DOUT+ is forced to logic low and output DOUT– is forced to logic high.
17	DOUT+	
19	1G_SEL	Selects the Data Rate of the Low Speed ND: Floating or Low: 2.5G ND selected (default). High: 1.25G ND selected. Performance with 1.25G selected is similar to 2.5G performance. Contact Microchip for more detail on 1.25G performance.

TABLE 3-1:   PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
20	POL_CTRL	Signal Polarity Control. LVTTL input with internal 25 kΩ pull-down resistor to invert the polarity of DOUT+/–. POL_CTRL = LOW (left open, tied to GND or low-level signal applied): No polarity inversion. POL_CTRL = HIGH (tied to VCC or high-level signal applied): DOUT– becomes the true output and DOUT+ becomes the complementary output.
21	LOS/SD_SEL	LVTTL input with internal 25 kΩ pull-down resistor. Allows the user to select between whether LOS or SD is outputted on the LOS/SD pin. Also controls the polarity of the JAM input. When SD (regardless of the noise discriminator status) is selected, JAM is active-high and LOS/SD operates as signal detect. Conversely, when LOS is selected, JAM is active-low and LOS/SD operates as loss-of-signal. SD selected if left open, tied to GND, or low LVTTL applied. LOS selected if tied to VCC or high LVTTL applied.
22	LOS/SD_LVL	Voltage Input. Sets the Loss-of-Signal/Signal Detect Threshold Level. A resistor (R_{LOSLVL}) from this pin to VCC or a DC signal between $V_{CC} - 0.6V$ and $V_{CC} - 1.0V$ sets the threshold for the data input amplitude at which LOS/SD will be asserted (resp. deasserted).
23	LOS/SD	LVTTL Output. Signal Detect (SD) asserts high when the data input amplitude rises above the threshold set by LOS/SD_LVL. Conversely, loss-of-signal (LOS) deasserts low when the data input amplitude rises above the threshold set by LOS/SD_LVL.
24	JAM	LVTTL Input. This JAM input acts as a squelch function and switches its polarity depending on LOS/SD_SEL status. When LOS is selected, this pin is active-high. When SD is selected, this pin is active-low. To create a squelch function, connect JAM to LOS/SD. When JAM disables the device, output DOUT+ is forced to logic low and output DOUT– is forced to logic high. Note that this input is internally connected to a 25 kΩ pull-up resistor. In case LOS is selected without using the squelch function, it has to be connected to a low level to enable the output.
EPAD	ePAD	Exposed thermal pad. Must be soldered to PCB plane connected to the negative supply rail. The recommended via array is needed to remove heat from the device.

SY88029L
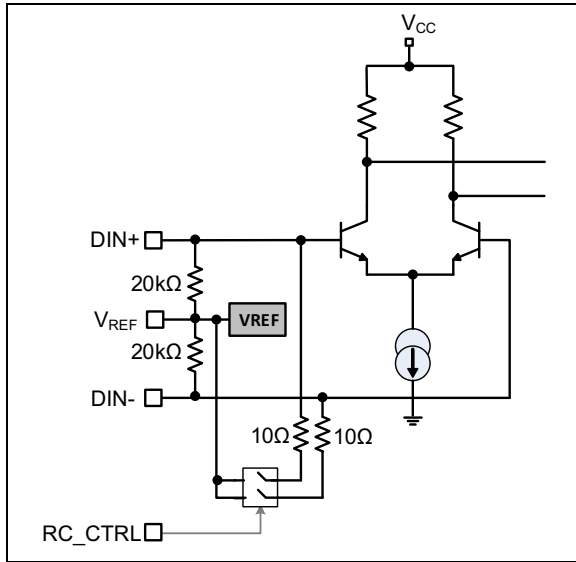
4.0   INPUT AND OUTPUT STRUCTURES
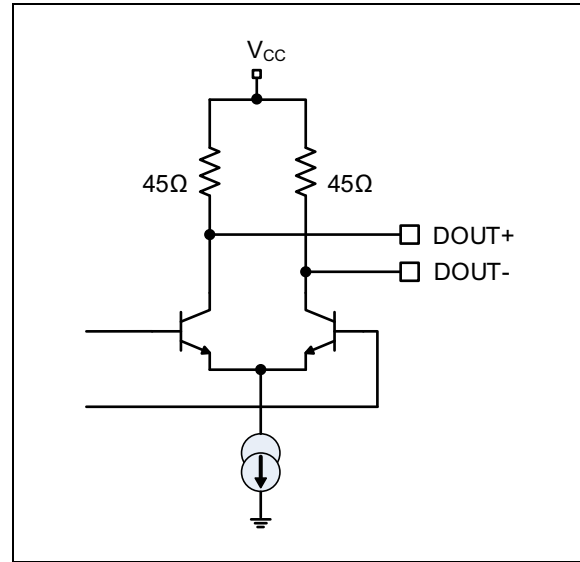

FIGURE 4-1:   Input Stage, AC-Coupled
Only.

FIGURE 4-2:   Output Stage.

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5.0   FUNCTIONAL DESCRIPTION

The SY88029L is a high-sensitivity, high-bandwidth, burst-mode, dual-rate 2.5G/10G limiting post amplifier with integrated rate detect function designed for use in XG-PON, XGS-PON, and NG-PON2 OLT transceivers. It operates from a single +3.3V power supply across the extended temperature range of –40°C to +95°C.

The device features a wide bandwidth input buffer that can detect signals with data rates ranging from well below 2.5 Gbps to 12.5 Gbps and amplitudes as small as 5 mV$_{PP}$. Figure 5-1 shows the allowed input voltage swing.
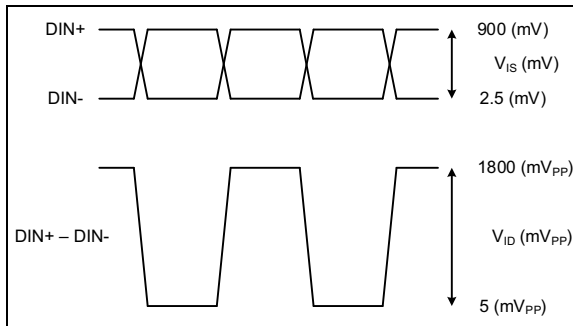
FIGURE 5-1: V_{IS} and V_{ID} Definitions.

The signal coming out from the input buffer continues through the limiting amplifier block, a pre-driver block, and the output buffer. The part has two modes of operation depending on if the noise discriminator (ND) incorporated in the signal detect block is enabled or disabled.

If ND is disabled, the amplifier let signals at any data rate from DC to 12.5 Gbps go through.

If ND is enabled (rate detect mode), the part will let only 2.5G and 10G data rate signals, whichever is detected (with a certain margin), go through.

The SY88029L has a selectable LOS or SD status output signal that can be fed back to the JAM input to perform the squelch function for output stability in the absence of a valid input signal. LOS/SD_LVL sets the sensitivity of the input amplitude detection.

In applications where the noise is not evenly distributed between the high levels and the low levels of the signal, the zero crossing point (decision threshold) can be adjusted using the CPA pin to optimize the BER performance of the link.

The part also features output signal amplitude adjustment and pre-emphasis. The output swing can be programmed using SW_CTRL1 and SW_CTRL2. Output pre-emphasis is activated by applying a DC voltage between 0V and 2.5V at the PELVL pin. Figure 2-6 and Figure 2-7 show output swing vs SW_CTRL1 and SW_CTRL2 settings.

5.1   Input Amplifier/Buffer

Figure 4-1 shows a simplified schematic of the input stage of SY88029L. The SY88029L has a 20 kΩ input termination to VREF in parallel with a switch that can be closed by setting RC_CTRL to high and shorting the 20 kΩ with a 10Ω resistor to bring the RC time constant much lower to allow for a fast receiver settling when the input data switches from a strong burst to a weak burst and vice versa. The high sensitivity of the input stage allows signals as small as 5 mV$_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as 1800 mV$_{PP}$.

5.2   Output Buffers

The SY88029L has a CML output buffer designed to drive 50Ω impedance transmission lines and is internally terminated with 45Ω to VCC. Figure 4-2 shows simplified schematics of the output stage.

5.3   Signal Detect/Loss-of-Signal

The SY88029L generates a user-selectable signal detect (SD) or loss-of-signal (LOS) TTL output. LOS is used to determine whether the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOS/SD_LVL and deasserts low otherwise. LOS can be fed back to the JAM input to perform the squelch function to maintain output stability under a LOS condition deasserting the true output signal low without removing the input signals. Typically, 3.5 dB of LOS hysteresis is provided to prevent chattering.

When SD output is selected (LOS/SD_SEL set to low) on the LOS/SD pin, SD is asserted when the differential input signal amplitude exceeds the level set by the LOS/SD_LVL. The JAM operation is inverted when SD is selected.

5.4   Signal Detect/Loss-of-Signal Level Setting

The threshold of the input amplitude detection can be set by either connecting an external resistor (R$_{LOSLVL}$) between VCC and the LOS/SD_LVL pin or by applying a voltage between V$_{CC}$ – 0.6V and V$_{CC}$ – 1.0V to that pin.

5.5   Hysteresis

To prevent LOS/SD signal from chattering when the amplitude of input signal oscillates above and below the sensitivity level set by the voltage level at the LOS/SD_LVL pin, the SY88029L provides typically 3.5 dB LOS electrical hysteresis, which is defined as 20log(VIN$_{LOS\_Deassert}$ ÷ VIN$_{LOS\_Assert}$). Because the relationship between the voltage output of the ROSA to optical power at its input is linear, the optical hysteresis is typically half of the electrical hysteresis reported in

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the data sheet. In practice, the ratio between electrical and optical hysteresis is found to be between 1.5 and 1.8. Thus, 3.5 dB of electrical hysteresis corresponds to an optical hysteresis within the range of 1.7 dB to 1.9 dB.
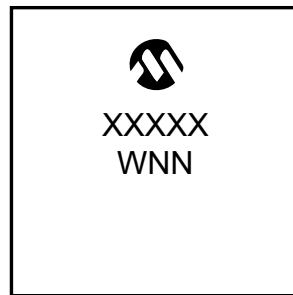
5.6   Signal Crossing Point Adjustment

To optimize the decision threshold level, and so the BER of the optical link where the noise is unevenly distributed between the high and the low levels, the SY88029L provides two pins for output signal crossing point adjustment (decision threshold) control.

The output signal crossing can be adjusted by setting the CPA_CTRL pin to high and applying a voltage between 0V and 2.5V to the CPA pin. 0V will set the crossing to 35% and 2.5V will set it to 75%.

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24-Lead QFN 4 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
24 LEAD QFN 4x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN44-24LD-PL-1	**UNIT**	MM

Pin 1 Dot
By marking

4.00 BSC

4.00 BSC

1
2
3

TOP VIEW
NOTE: 1, 2, 3

2.50±0.05
Exp. DAP

PIN #1 ID

0.400±0.05

R0.20

0.25±0.05

2.50±0.05
Exp. DAP

0.500 BSC

2.5000
Ref.

BOTTOM VIEW
NOTE: 1, 2, 3

0.850±0.050

0.05 C

SEATING PLANE

0.203±0.025

0.02 +0.03 -0.02

SIDE VIEW
NOTE: 1, 2, 3

0.48±0.02

0.50 BSC

0.23±0.02

2.6±0.02

3.24±0.02

4.20±0.05
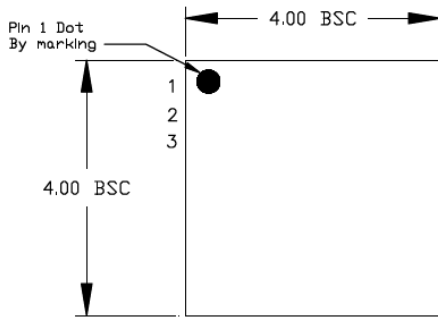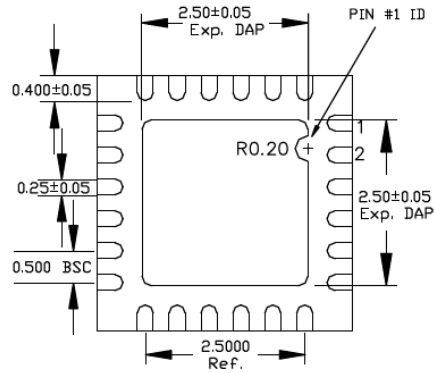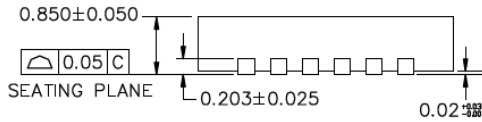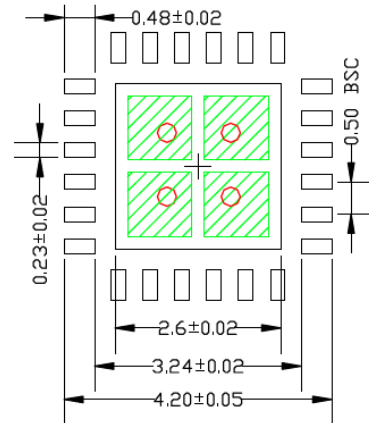
RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA, SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA.   SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (July 2018)

• Initial release of SY88029L as Microchip data sheet DS20006056A.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	XX
Device	Voltage Option	Package	Temperature	Special Processing

Device:	SY88029:	2.5G/10G Dual-Rate Burst Mode Limiting Post Amplifier for XG-PON, XGS-PON, NG-PON2 OLT Transceiver
Voltage Option:	L =	3.3V Only
Package:	M =	24-Lead 4 mm x 4 mm QFN
Temperature:	G =	–40°C to +95°C
Special Processing:	Blank = TR =	91/Tube 500/Reel

Examples:

a) SY88029LMG: SY88029, 3.3V Voltage Option, –40°C to +95°C Temp. Range, 24-Lead QFN, 91/Tube

b) SY88029LMG-TR: SY88029, 3.3V Voltage Option, –40°C to +95°C Temp. Range, 24-Lead QFN, 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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NOTES:

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