
Getting Started with the ATA8201/ATA8202 Evaluation Kit

1. Introduction

ATA8201/ATA8202 is a transparent receiver which can be used processing the data for two different applications, which contain different data rate as well as modulation type, Amplitude Shift Keying (ASK) or Frequency Shift Keying (FSK). For handling the different applications ATA8201/ATA8202 can be switched in a very short time between ASK and FSK modulation types and of course between four data rate ranges.

For evaluation purposes of ATA8201/ATA8202, the board ATA5745/ATA5746-EK is designed. With the evaluation board the receiver can be evaluated without any micro-controller since there are 8 switches implemented for the receiver's setting. The board is assembled for an operating voltage of 3V. To operate with power supply of 5V the on board external circuitry of the receiver's power supply must be changed (for this issue please refer to the datasheet) The RF input is matched to 50Ω. This simplifies the verification of the input stage with the standard RF instrument.

[Figure 1-1 on page 2](#) is a photo of an assembled board, [Figure 1-2 on page 2](#) shows the layout of the top layer, and [Figure 1-3 on page 3](#) shows the allocation of the test pins (Jx, where x is an index) on the board. For each test pin there is a ground pin available in order to simplify measurement with an oscilloscope's probe. When measuring the clock signal, the load capacitance of the probe has to be taken to account. [Table 1-1 on page 3](#) shows the information important for measurement purposes. The bill of materials for the board is listed in [Table 1-4 on page 4](#).



ATA8201/ ATA8202 Evaluation Kit

Application Note

9112A-AUTO-12/07



Figure 1-1. Evaluation Board of the ATA5745/ATA5746, which is also used for Evaluating ATA8201/ATA8202

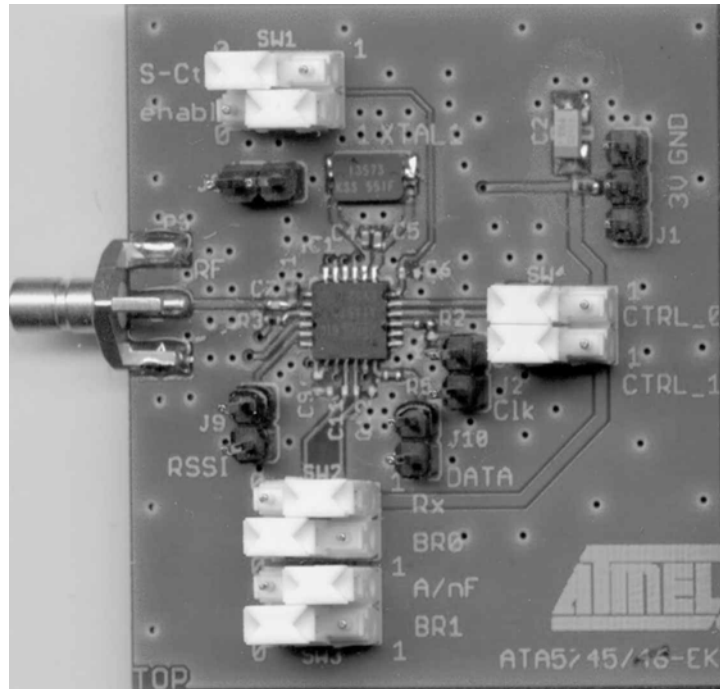


Figure 1-2. Top Layer Layout of the ATA5745/ATA5746-EK (ATA8201/ATA8202-EK)

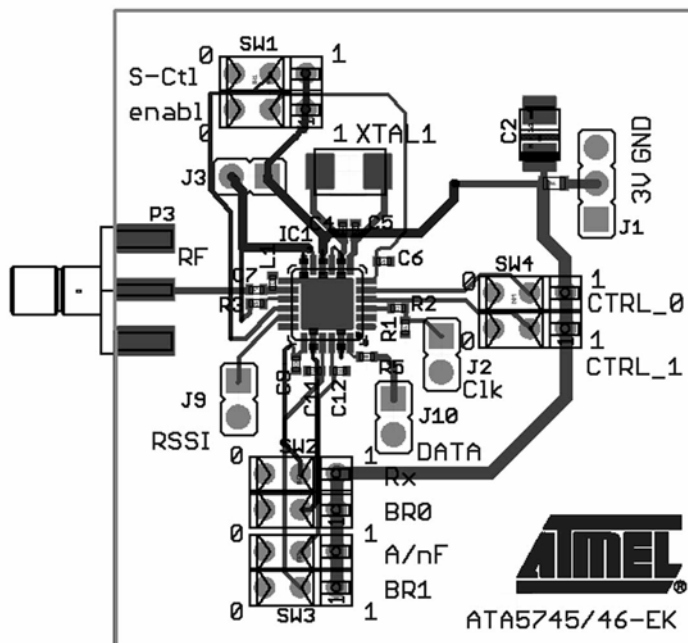
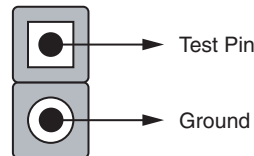


Table 1-1. Mapping of the Board Components and Designators to the Pins of ATA8201/ATA8202

| Board Components | Designator and Description | The Corresponding Pin of the ATA8201/ATA8202 |
|------------------|--|--|
| SW1 | S-Ctl, <i>enabl</i> | SENSE_CTRL, ENABLE |
| SW2 | Rx, BR0 | RX, BR0 |
| SW3 | A/nF, BR1 | ASK_NFSK, BR1 |
| SW4 | CTRL_0, CTRL_1 | CLK_OUT_CTRL_0, CLK_OUT_CTRL_1 |
| J1 | Power supply of the board, $V_S = 3V$ | |
| J2 | Test pin to measure the clock signal. Connected to pin CLK_OUT over a 0Ω resistor (R2) (see Figure 1-3) | CLK_OUT |
| J3 | The connector between VS3 and VS5 | VS5V, VS3V_AVCC |
| J9 | Test pin to measure the RSSI signal (see Figure 1-3) | RSSI |
| J10 | Test pin to measure the demodulated data. Connected to pin DATA_OUT over a 0Ω resistor (R5) (see Figure 1-3) | DATA_OUT |

Note: The switches are double switches. One switch component (SWx) consists of two switches.

Figure 1-3. Allocation of the Row Connectors (Test Pins) for Measurement Assembly



The following steps need to be followed to start working with the evaluation board:

1. Activate the 3V power supply.
2. Set switches *enabl* and *Rx* to “1” in order to start the receiver in receiving mode.
3. Set switches *BR0* and *BR1* according to [Table 1-2](#) for the desired data rate to be processed by the receiver.

Table 1-2. The Receiver’s Bit Rate Depends on the Combination of *BR0* and *BR1*

| BR1 | BR0 | BR_Range | Recommended Bit Rate (Manchester) |
|-----|-----|-----------|--|
| 0 | 0 | BR_Range0 | 1 kBit/s to 2.5 kBits/s |
| 0 | 1 | BR_Range1 | 2 kBits/s to 5 kBits/s |
| 1 | 0 | BR_Range2 | 4 kBits/s to 10 kBits/s |
| 1 | 1 | BR_Range3 | 8 kBits/s to 10 kBits/s (ASK) 8 kBits/s to 20 kBits/s (FSK) |



4. Set switch *A/nF* as desired to set the modulation type of the receiver: “1” for ASK, or “0” for an FSK-modulated signal.
5. Set switch *S-Ctl* as desired for the sensitivity reduction functionality. Set *S-Ctl* to LOW for normal sensitivity or HIGH for the sensitivity reduction functionality. The resistor on pin SENSE (R3) determines the value of the reduction. For more information, refer to the datasheet.
6. Set *CTRL_0* and *CTRL_1* as shown in Table 1-3 for the frequency of the clock signal to be measured on test pin J2.

Table 1-3. The Functionality of the Pin CLOCK_OUT Depending on the Logic Combination of the Pins CTRL_0 and CTRL_1

| CTRL_1 | CTRL_0 | Function |
|--------|--------|-------------------------------|
| 0 | 0 | Pin CLK_OUT is switched off |
| 0 | 1 | $f_{CLK_OUT} = f_{XTO} / 3$ |
| 1 | 0 | $f_{CLK_OUT} = f_{XTO} / 6$ |
| 1 | 1 | $f_{CLK_OUT} = f_{XTO} / 12$ |

Note: f_{XTO} at 433 MHz = 13.57375 MHz, f_{XTO} at 315 MHz = 13.1433 MHz

Table 1-4. Bill of Materials of the ATA8201/ATA8202-EK

| Components | Pcs | 315 MHz | 433 MHz | Value | Tolerance | Material/Series | Housing | Manufacturer/ Distributor |
|--------------------------------|------|---------|---------|---------------|-----------|-------------------|--------------------------|----------------------------------|
| IC1 | 1 | x | | ATA8202 | | | QFN24 | Atmel® |
| | | | x | ATA8201 | | | | |
| R2, R3, R5 | 4 | x | x | 0Ω | | | 0402 | Murata® |
| C2 | 1 | x | x | 4.7 μF | | | | |
| C4, C5 | 2 | x | x | 18 pF | | | 0402 | |
| C51, C52, C53 | 3 | x | x | 10 nF | | | 0402 | |
| C7 | 1 | x | x | 2.2 pF | | X7R | 0402 | |
| C54 | 1 | x | x | 15 nF | | X7R | 0402 | |
| L1 | 1 | x | | 68 nH | Q = 20 | 0402CS | 0402 | Coilcraft® |
| | | | x | 36 nH | Q = 15 | 0402CS | 0402 | Coilcraft |
| XTAL1 | 1 | x | | 13.1433 MHz | | | CX-53G | Kyocera® Kinseki |
| | | | x | 13.57375 MHz | | | | |
| SW1, SW2, SW3, SW4 | 4 | x | x | | | JSK9-1G2-G0 | | ITW/PANCON - Heilind Electronics |
| J2, J3, J9, J10 | 4 | x | x | Row connector | | 800-10-012-10-001 | 2 pins/ 0.1 in. pitch | CAB |
| J1 | 1 | x | x | Row connector | | 800-10-012-10-001 | 3 pins/ 0.1 in. pitch | CAB |
| P3 | | | | SMB connector | | Radiall® | | Radiall |
| R1, C6, C9, C11, C12, C55, FB1 | n.m. | | | | | | | |



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