

Data Sheet

The SST12LP18E is a versatile power amplifier based on the highly-reliable InGaP/GaAs HBT technology. The SST12LP18E is a 2.4 GHz high-efficiency Power Amplifier designed in compliance with IEEE 802.11b/g/n/ac applications. It typically provides 25 dB gain with 32% power-added efficiency, while meeting 802.11g spectrum mask at 21.5 dBm. The SST12LP18E can be configured for high-linearity for 802.11ac operation or for high-power, high-efficiency operation. This power amplifier also features easy board-level usage along with high-speed power-up/down control through a single reference voltage pin and is offered in a 8-contact XSON package.

### Features

#### • High gain:

- Typically 25 dB gain across 2.4~2.5 GHz
- High linear output power:
  - ->26 dBm P1dB
  - Single-tone measurement
  - Please refer to "Absolute Maximum Stress Ratings" on page 5
  - Meets 802.11g OFDM ACPR requirement up to 21.5 dBm
  - Meets 802.11b ACPR requirement up to 22.5 dBm
  - ~3% added EVM up to 18 dBm for 54 Mbps 802.11g signal
  - 17 dBm at 1.8% EVM, 802.11ac, 256 QAM, 2.4 GHz
- High power-added efficiency/Low operating current for 802.11b/g/n applications
  - ~32%/135 mA @  $P_{OUT}$  = 21.5 dBm for 802.11g – ~36%/150 mA @  $P_{OUT}$  = 22.5 dBm for 802.11b
- Single-pin low I<sub>REF</sub> power-up/down control

 $-I_{REF} < 2 \text{ mA}$ 

- Low idle current for high-efficiency operation
  - ~50 mA I<sub>CQ</sub>
- High-speed power-up/down control
  - Turn on/off time (10%- 90%) <100 ns
  - Typical power-up/down delay with driver delay included <200 ns</li>

- Low shut-down current (~2 μA)
- Limited variation over temperature -~1 dB gain/power variation between -20°C to +85°C
- Excellent on-chip power detection ->15 dB dynamic range on-chip power detection - Temperature and VSWR insensitive
- Simple output matching
- Packages available
  - 8-contact XSON 2mm x 2mm
- All non-Pb (lead-free) devices are RoHS compliant

### Applications

- WLAN (IEEE 802.11b/g/n/ac)
- Home RF
- Cordless phones
- 2.4 GHz ISM wireless equipment



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### **Product Description**

The SST12LP18E is a versatile power amplifier based on the highly-reliable InGaP/GaAs HBT technology.

The SST12LP18E is a 2.4 GHz high-efficiency Power Amplifier designed in compliance with IEEE 802.11b/g/n/ac applications. It typically provides 25 dB gain with 32% power-added efficiency (PAE) @ POUT = 21.5 dBm for 802.11g and 36% PAE @ POUT = 22.5 dBm for 802.11b.

The SST12LP18E has excellent linearity, typically ~3% added EVM at 18 dBm output power which is essential for 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 21.5 dBm. SST12LP18E can also be configured for high-linearity with EVM <1.8% at typically 17 dBm for 802.11ac operation.

The SST12LP18E also features easy board-level usage along with high-speed power-up/down control through a single combined reference voltage pin. Ultra-low reference current (total  $I_{REF} \sim 2$  mA) makes the SST12LP18E controllable by an on/off switching signal directly from the baseband chip. These features, coupled with low operating current, make the SST12LP18E ideal for the final stage power amplification in battery-powered 802.11b/g/n/ac WLAN transmitter applications.

The SST12LP18E has an excellent on-chip, single-ended power detector, which features wide-range (>15 dB) with dB-wise linear operation. The excellent on-chip power detector is both temperature and VSWR insensitive; therefore, it provides a reliable solution to board-level power control.

The SST12LP18E is offered in 8-contact XSON package. See Figure 2 for pin assignments and Table 1 for pin descriptions.



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### **Functional Blocks**

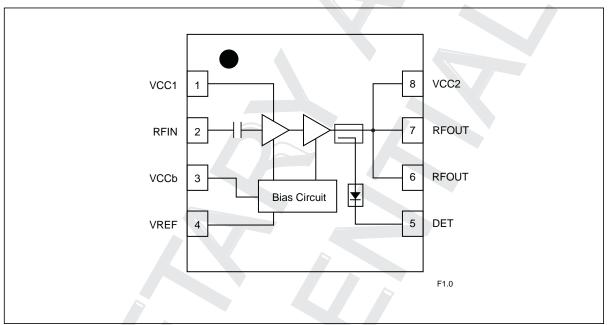


Figure 1: Functional Block Diagram



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## **Pin Assignments**

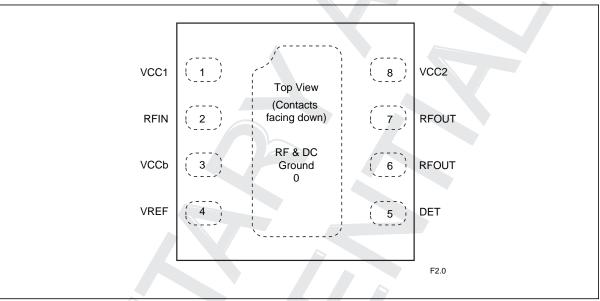


Figure 2: Pin Assignments for 8-contact XSON

### **Pin Descriptions**

Table 1. Thir Description							
Symbol	Pin No.	Pin Name	Type <sup>1</sup>	Function			
GND	0	Ground		Low inductance GND pad			
V <sub>CC1</sub>	1	Power Supply	PWR	Power supply, 1 <sup>st</sup> stage			
RF <sub>IN</sub>	2		I	RF input, DC decoupled			
V <sub>CCb</sub>	3	Power Supply	PWR	Supply voltage for bias circuit			
VREF	4		PWR	1 <sup>st</sup> and 2 <sup>nd</sup> stage idle current control			
Det	5		0	On-chip power detector			
RFOUT	6		0	RF output			
RFOUT	7		0	RF output			
V <sub>CC2</sub>	8	Power Supply	PWR	Power supply, 2 <sup>nd</sup> stage			

#### Table 1: Pin Description

1. I=Input, O=Output

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### **Electrical Specifications**

The DC and RF specifications for the power amplifier are specified below. Refer to Table 3 for the DC voltage and current specifications. Refer to Figures 3 through 13 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pin 2 (P <sub>IN</sub> )	+5 dBm
Average output power (P <sub>OUT</sub> ) <sup>1</sup>	. +26 dBm
Supply Voltage at pins 1, 3, and 8(V <sub>CC</sub> )0.3	3V to +4.2V
Reference voltage to pin 4 (V <sub>REF</sub> )0.3	3V to +3.3V
DC supply current (I <sub>CC</sub> ) <sup>2</sup>	300 mA
Operating Temperature (T <sub>A</sub> )40°	C to +85°C
Storage Temperature (T <sub>STG</sub> )40°C	; to +120ºC
Maximum Junction Temperature (T <sub>J</sub> )	+150⁰C
Surface Mount Solder Reflow Temperature 260°C for 1	10 seconds
<ol> <li>Never measure with CW source. Pulsed single-tone source with &lt;50% duty cycle is recommended. Excee imum rating of average output power could cause permanent damage to the device.</li> </ol>	ding the max-
2. Measured with 100% duty cycle 54 Mbps 802 11g OEDM Signal	

#### Table 2: Operating Range

	Range	Ambient Temp	V <sub>cc</sub>
Industrial -40°C to +85°C 3.3V	Industrial	-40°C to +85°C	3.3V

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#### Table 3: DC Electrical Characteristics at 25°C for High-Linearity Configurations<sup>1</sup>

Symbol	Parameter			Max.	Unit
Vcc	Supply Voltage at pins 1,3,and 8	3.0	3.3	3.6	V
I <sub>CQ</sub>	Idle current to meet EVM ~1.8% @ 17 dBm Output Power with 802.11g OFDM 54 Mbps signal		110		mA
Icc	Current Consumption @ 18 dBm Output Power with 802.11g OFDM 54 Mbps signal		140		
	Current Consumption to meet 802.11g OFDM 6 Mbps Spectrum mask @ 21.5 dBm Output Power				mA
	Current Consumption to meet 802.11b DSSS 1 Mbps Spectrum mask @ 22.5 dBm Output Power		180		mA
V <sub>REG</sub>	Reference Voltage with $0\Omega$ resistor	2.7	2.8	2.9	V
<b>-</b>				Т3.	1 75003

1. See Figure 8

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Symbol	Parameter	Min.	Тур	Max.	Unit
V <sub>CC</sub>	Supply Voltage at pins 1,3,and 8	3.0	3.3	3.6	V
I <sub>CQ</sub>	Idle current to meet EVM ~3% @ 18 dBm Output Power with 802.11g OFDM 54 Mbps signal		50		mA
	Current Consumption @ 18 dBm Output Power with 802.11g OFDM 54 Mbps signal	7/	95		
I <sub>CC</sub>	Current Consumption to meet 802.11g OFDM 6 Mbps Spectrum mask @ 21.5 dBm Output Power		135		mA
	Current Consumption to meet 802.11b DSSS 1 Mbps Spectrum mask @ 22.5 dBm Output Power		150		mA
V <sub>REG</sub>	Reference Voltage with 360Ω resistor	2.7	2.8	2.9	V

#### Table 4: DC Electrical Characteristics at 25°C for High-Efficiency Configurations<sup>1</sup>

1. See Figure 14

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#### Table 5: RF Electrical Characteristics at 25°C

Symbol	Parameter	Min.	Тур	Max.	Unit
F <sub>L-U</sub>	Frequency range	2412		2484	MHz
G	Small signal gain	24	25		dB
G <sub>VAR1</sub>	Gain variation over band (2412–2484 MHz)			±0.5	dB
G <sub>VAR2</sub>	Gain ripple over channel (20 MHz)		0.2		dB
	EVM@ 18 dBm Output Power with 802.11g OFDM 54 Mbps signal <sup>1</sup>		3.0		%
EVM	EVM@ 17 dBm Output Power with 802.11ac 20 MHz BW <sup>2</sup>		1.8		%
POUT	Output Power to meet 802.11g OFDM 6 Mbps Spectrum mask	20.5	21.5		dBm
	Output Power to meet 802.11b DSSS 1 Mbps Spectrum mask	21.5	22.5		dBm
2f, 3f, 4f, 5f	Harmonics at 23 dBm, without external filters			-30	dBc
			•		T5.2 7500

1. See Figure 14

2. See Figure 8

#### Table 6: Typical Performance with Different Bias Options for High-Efficiency Configuration

V <sub>REG</sub> (V)	<b>R1<sup>1</sup> (</b> Ω <b>)</b>	I <sub>CQ</sub> <sup>2</sup> (mA)	I <sub>CC</sub> @ P <sub>OUT</sub> = 18 dBm <sup>2</sup> (mA)	Typical Performance with Each Biased Option
2.85	500	45	95	Meet added EVM < 3% up to 18 dBm output power at -40°C
2.80	360	50	95	Meet added EVM < 3% up to 18 dBm output power at -40°C
2.70	180	50	95	Meet added EVM < 3% up to 18 dBm output power at -20°C
2.70	33	72	110	Meet added EVM < 3% up to 18 dBm output power at -40°C
2.70	0	82	120	Meet added EVM < 3% up to 18 dBm output power at -40°C

1. See Figure 14

2. At room temperature

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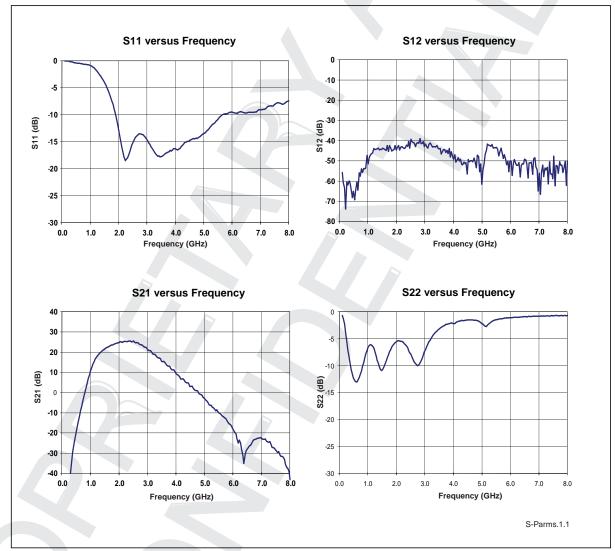


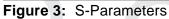
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### **Typical Performance Characteristics**

Test Conditions:  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified







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### High-Linearity Configuration for 802.11b/g/n/ac

**Typical Performance Characteristics** 

Test Conditions:  $V_{CC}$  = 3.3V,  $V_{REF}$  = 2.8V,  $T_A$  = 25°C, 54 Mbps 802.11g OFDM Signal; Equalizer Training Setting using Channel Estimation Sequence Only

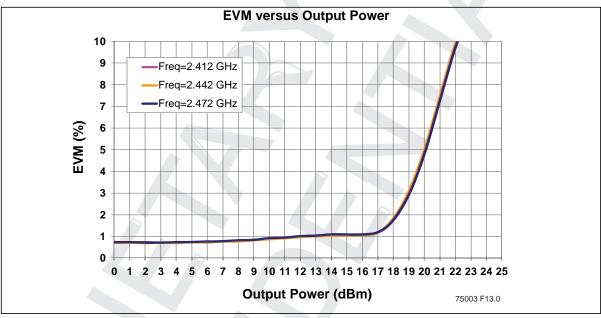


Figure 4: EVM versus Output Power

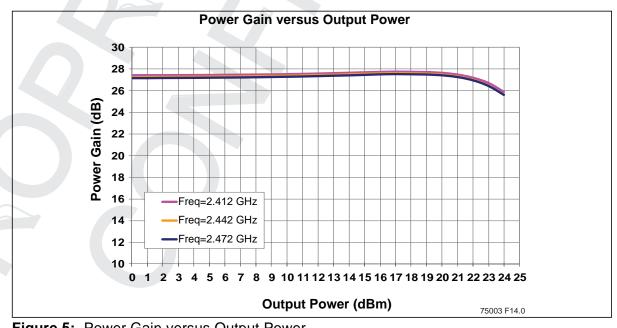


Figure 5: Power Gain versus Output Power



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## **High-Linearity Configuration (continued)**

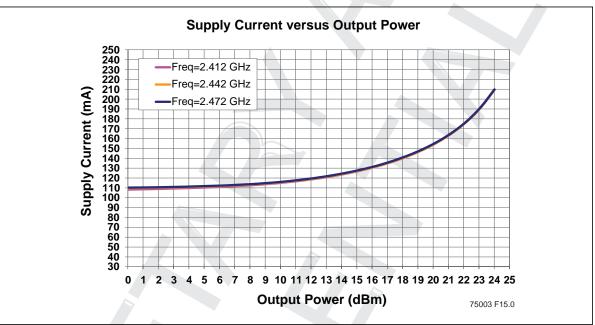
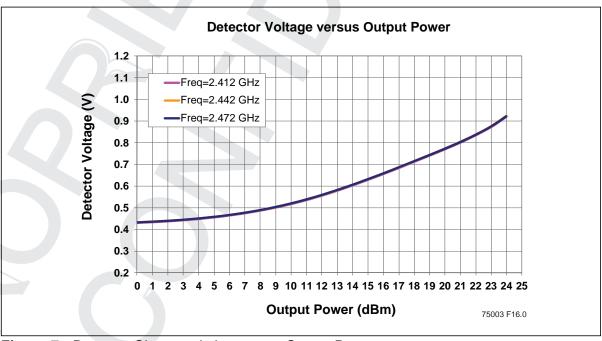


Figure 6: Total Current Consumption for 802.11g operation versus Output Power



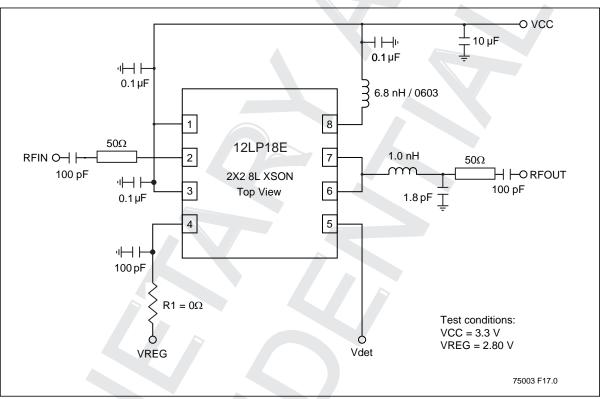


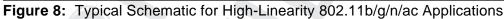


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## High-Linearity Configuration (continued)







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### High-Efficiency Configuration for 802.11b/g/n Operation

**Typical Performance Characteristics** 

Test Conditions:  $V_{CC}$  = 3.3V,  $V_{REF}$  = 2.8V,  $T_A$  = 25°C, 54 Mbps 802.11g OFDM Signal; Equalizer Training Setting using Channel Estimation Sequence Only

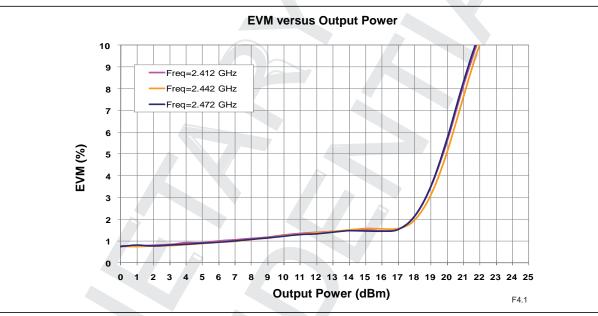


Figure 9: EVM versus Output Power

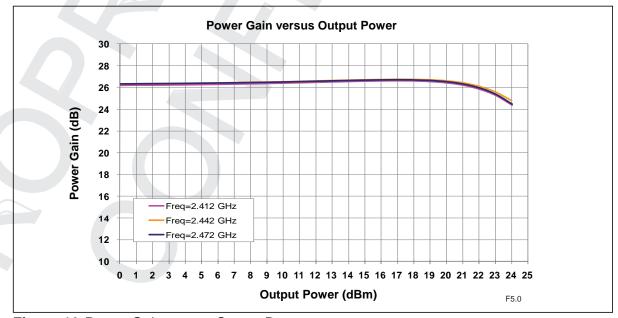


Figure 10: Power Gain versus Output Power



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## **High-Efficiency Configuration (continued)**

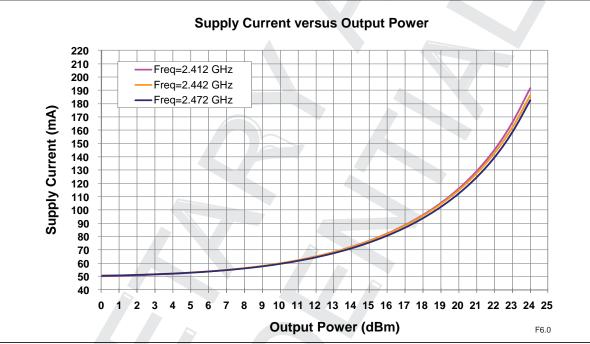
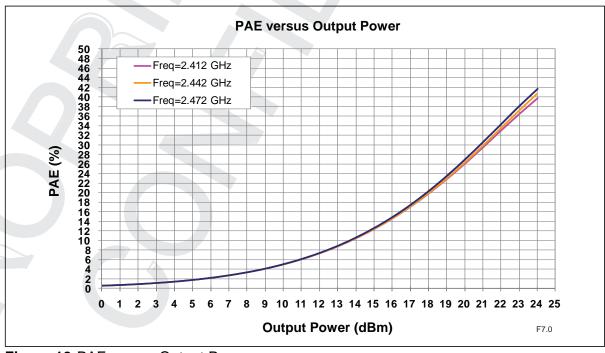


Figure 11: Total Current Consumption for 802.11g operation versus Output Power







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## **High-Efficiency Configuration (continued)**

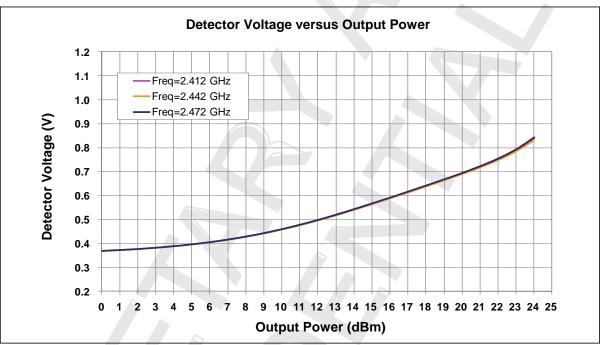


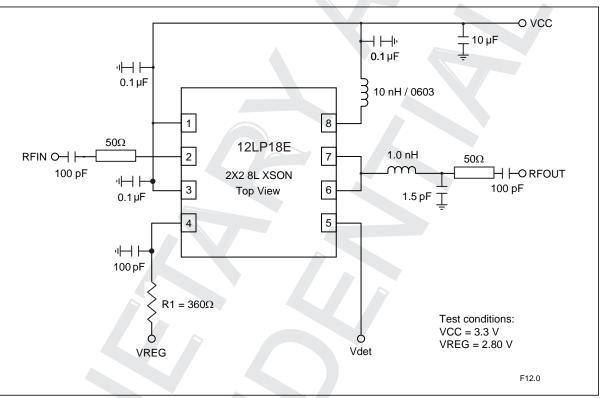
Figure 13: Detector Characteristics versus Output Power

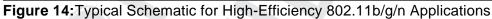


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## **High-Efficiency Configuration (continued)**





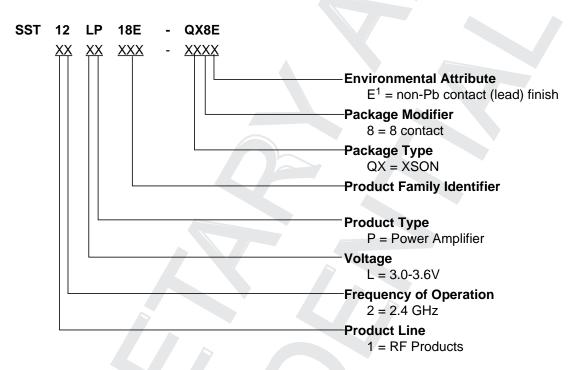




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### **Product Ordering Information**

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1. Environmental suffix "E" denotes non-Pb solder. SST non-Pb solder devices are "RoHS Compliant".

#### Valid combinations for SST12LP18E

SST12LP18E-QX8E

### SST12LP18E Evaluation Kits

SST12LP18E-QX8E-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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## Packaging Diagrams

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#### SIDE VIEW **BOTTOM VIEW** TOP VIEW 2.00 1.55 See notes ±0.10 3 and 4 Pin #1 ⊢ Pin # 1 (laser 1.60 engraved 2.00 see note 2) 0.40 BSC ±0.10 0.75 0.2 0.08 0.05 Max 0.3 <u>0.50</u> 0.41 1mm 8-xson-2x2-QX8-4.0 Note: 1. Similar to JEDEC JEP95 XQFN/XSON variants, though number of contacts and some dimensions are different. 2. The topside pin #1 indicator is laser engraved; its approximate shape and location is as shown. 3. From the bottom view, the pin #1 indicator may be either a curved indent or a 45-degree chamfer. 4. The external paddle is electrically connected to the die back-side and to $\mathsf{V}_{SS}.$ This paddle must be soldered to the PC board; it is required to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential will result in shorts and electrical malfunction of the device. 5 Untoleranced dimensions are nominal target dimensions. 6. All linear dimensions are in millimeters (max/min).

Figure 15:8-Contact Extremely-thin Small Outline No-lead (XSON) SST Package Code: QX8

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#### Table 7: Revision History

Revision		Description			
А	•	Initial release of data sheet			
В	•	• Revised "Electrical Specifications" on page 5 from 4.0V max stress to 4.6V			
	Updated Figure 9 on page 11 to show "sequence only" EVM response				
С	Added Figures 9-8 on pages 11-10 to provide High-Linearity information		Jul 2012		
	Updated Table 5 on page 6				
	•	Updated Figure 15 on page 16 to reflect new pin 1 indicator			
	•	Clarified Features on page 1			

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Memory sizes denote raw storage capacity; actual usable capacity may be less.

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