



# MCP14E9/10/11

## 3.0A Dual High-Speed Power MOSFET Driver With Enable

### Features

- High Peak Output Current: 3.0A (typical)
- Independent Enable Function for Each Driver Output
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - $t_R$ : 14 ns with 1800 pF load (typical)
  - $t_F$ : 17 ns with 1800 pF load (typical)
- Short Delay Times:
  - $t_{D1}$ : 45 ns (typical)
  - $t_{D2}$ : 45 ns (typical)
- Low Supply Current:
  - With Logic '1' Input/Enable – 1 mA (typical)
  - With Logic '0' Input/Enable – 300  $\mu$ A (typical)
- Latch-up Protected: Passed JEDEC JESD78A
- Logic Input will Withstand Negative Swing, up to 5V
- Space-Saving Packages:
  - 8-Lead SOIC, PDIP, 6x5 DFN

### Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Motor and Solenoid Drive

### General Description

The MCP14E9/10/11 devices are high-speed MOSFET drivers, capable of providing 3.0A of peak current. The dual inverting, dual non-inverting and complementary outputs are directly controlled from either TTL or CMOS (3V to 18V). These devices also feature low shoot-through current, near matched rise/fall times and propagation delays, which make them ideal for high switching frequency applications.

The MCP14E9/10/11 devices operate from a 4.5V to 18V single power supply and can easily charge and discharge 1800 pF of MOSFET gate capacitance. They provide low enough impedances, in both the ON and OFF states, to ensure the MOSFETs' intended state will not be affected, even by large transients.

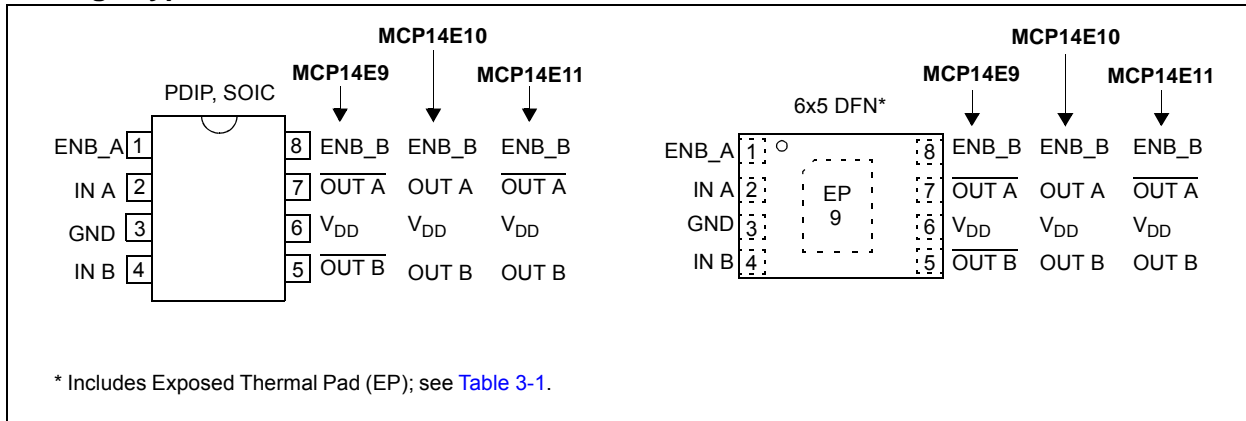
The additional control of the MCP14E9/10/11 outputs is allowed by the use of separate enable functions. The ENB\_A and ENB\_B pins are active-high and are internally pulled up to  $V_{DD}$ . The pins may be left floating for standard operation.

The MCP14E9/10/11 dual output 3.0A driver family is offered in both surface-mount and pin-through-hole packages with a  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature rating. The low thermal resistance of the thermally enhanced DFN package allows greater power dissipation capability for driving heavier capacitive or resistive loads.

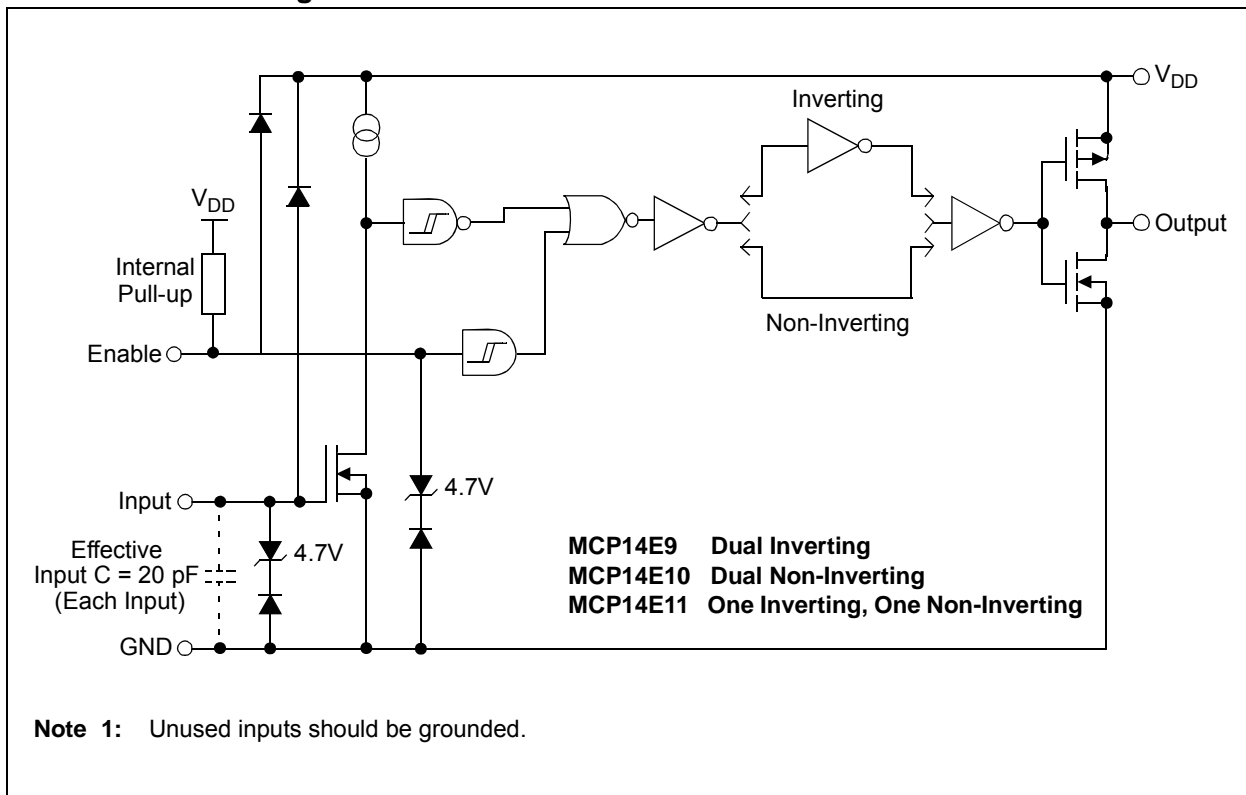
These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. The devices are fully latch-up protected when tested according to JEDEC JESD78A. All terminals are fully protected against Electrostatic Discharge (ESD), up to 4 kV (HBM) or 400V (MM).

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## Package Types



## Functional Block Diagram<sup>(1)</sup>



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....	+20V
Input Voltage .....	(V <sub>DD</sub> + 0.3V) to (GND – 5V)
Enable Voltage .....	(V <sub>DD</sub> + 0.3V) to (GND – 5V)
Input Current (V <sub>IN</sub> >V <sub>DD</sub> ).....	50 mA
Package Power Dissipation (T <sub>A</sub> = +50°C)	
8L-DFN .....	<b>Note 3</b>
8L-PDIP .....	1.12W
8L-SOIC .....	669 mW

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS<sup>(2)</sup>

Electrical Specifications: Unless otherwise indicated, T <sub>A</sub> = +25°C, with 4.5V ≤ V <sub>DD</sub> ≤ 18V.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input</b>						
Logic '1', High Input Voltage	V <sub>IH</sub>	2.4	1.5	—	V	
Logic '0', Low Input Voltage	V <sub>IL</sub>	—	1.3	0.8	V	
Input Current	I <sub>IN</sub>	-1	—	1	μA	0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>
Input Voltage	V <sub>IN</sub>	-5	—	V <sub>DD</sub> + 0.3	V	
<b>Output</b>						
High Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> – 0.025	—	—	V	DC Test
Low Output Voltage	V <sub>OL</sub>	—	—	0.025	V	DC Test
Output Resistance, High	R <sub>OH</sub>	—	4	7	Ω	I <sub>OUT</sub> = 10 mA, V <sub>DD</sub> = 18V
Output Resistance, Low	R <sub>OL</sub>	—	4	7	Ω	I <sub>OUT</sub> = 10 mA, V <sub>DD</sub> = 18V
Peak Output Current	I <sub>PK</sub>	—	3	—	A	V <sub>DD</sub> = 18V <sup>(2)</sup>
<b>Switching Time<sup>(1)</sup></b>						
Rise Time	t <sub>R</sub>	—	14	30	ns	Figure 4-1, Figure 4-2, C <sub>L</sub> = 1800 pF
Fall Time	t <sub>F</sub>	—	17	30	ns	Figure 4-1, Figure 4-2, C <sub>L</sub> = 1800 pF
Propagation Delay Time	t <sub>D1</sub>	—	45	55	ns	Figure 4-1, Figure 4-2
Propagation Delay Time	t <sub>D2</sub>	—	45	55	ns	Figure 4-1, Figure 4-2
<b>Enable Function (ENB_A, ENB_B)</b>						
High-Level Input Voltage	V <sub>EN_H</sub>	2.4	1.6	—	V	V <sub>DD</sub> = 12V, Low-to-High Transition
Low-Level Input Voltage	V <sub>EN_L</sub>	—	1.2	0.8	V	V <sub>DD</sub> = 12V, High-to-Low Transition
Hysteresis	V <sub>HYST</sub>	—	400	—	mV	
Enable Pull-up Impedance	R <sub>ENBL</sub>	0.7	1.6	3.0	MΩ	V <sub>DD</sub> = 14V, ENBL = GND
Enable Pin Leakage Current	I <sub>ENBL</sub>	—	10	—	μA	V <sub>DD</sub> = 12V, ENB_A = ENB_B = GND
Propagation Delay Time	t <sub>D3</sub>	—	35	65	ns	V <sub>DD</sub> = 12V, Figure 4-3
Propagation Delay Time	t <sub>D4</sub>	—	35	65	ns	V <sub>DD</sub> = 12V, Figure 4-3

**Note 1:** Switching times are ensured by design.

**2:** Tested during characterization, not production tested.

**3:** Package power dissipation is dependent on the copper pad area of the PCB.

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## DC CHARACTERISTICS<sup>(2)</sup> (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ , with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	4.5	—	18.0	V	
Supply Current	$I_{DD}$	—	1000	1800	$\mu\text{A}$	$V_{IN\_A} = 3\text{V}$ , $V_{IN\_B} = 3\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{High}$
	$I_{DD}$	—	600	900	$\mu\text{A}$	$V_{IN\_A} = 0\text{V}$ , $V_{IN\_B} = 0\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{High}$
	$I_{DD}$	—	800	1600	$\mu\text{A}$	$V_{IN\_A} = 3\text{V}$ , $V_{IN\_B} = 0\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{High}$
	$I_{DD}$	—	800	1600	$\mu\text{A}$	$V_{IN\_A} = 0\text{V}$ , $V_{IN\_B} = 3\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{High}$
	$I_{DD}$	—	600	1000	$\mu\text{A}$	$V_{IN\_A} = 3\text{V}$ , $V_{IN\_B} = 3\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{Low}$
	$I_{DD}$	—	300	450	$\mu\text{A}$	$V_{IN\_A} = 0\text{V}$ , $V_{IN\_B} = 0\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{Low}$
	$I_{DD}$	—	500	800	$\mu\text{A}$	$V_{IN\_A} = 3\text{V}$ , $V_{IN\_B} = 0\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{Low}$
	$I_{DD}$	—	500	800	$\mu\text{A}$	$V_{IN\_A} = 0\text{V}$ , $V_{IN\_B} = 3\text{V}$ , $\text{ENB\_A} = \text{ENB\_B} = \text{Low}$

- Note 1:** Switching times are ensured by design.  
**Note 2:** Tested during characterization, not production tested.  
**Note 3:** Package power dissipation is dependent on the copper pad area of the PCB.

## DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE)<sup>(2)</sup>

Electrical Specifications: Unless otherwise indicated, operating temperature range with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input</b>						
Logic '1', High Input Voltage	$V_{IH}$	2.4	—	—	V	
Logic '0', Low Input Voltage	$V_{IL}$	—	—	0.8	V	
Input Current	$I_{IN}$	-10	—	+10	$\mu\text{A}$	$0\text{V} \leq V_{IN} \leq V_{DD}$
<b>Output</b>						
High Output Voltage	$V_{OH}$	$V_{DD} - 0.025$	—	—	V	DC Test
Low Output Voltage	$V_{OL}$	—	—	0.025	V	DC Test
Output Resistance, High	$R_{OH}$	—	7	9	$\Omega$	$I_{OUT} = 10\text{ mA}$ , $V_{DD} = 18\text{V}$
Output Resistance, Low	$R_{OL}$	—	7	9	$\Omega$	$I_{OUT} = 10\text{ mA}$ , $V_{DD} = 18\text{V}$
<b>Switching Time<sup>(1)</sup></b>						
Rise Time	$t_R$	—	25	40	ns	Figure 4-1, Figure 4-2, $C_L = 1800\text{ pF}$
Fall Time	$t_F$	—	25	40	ns	Figure 4-1, Figure 4-2, $C_L = 1800\text{ pF}$
Propagation Delay Time	$t_{D1}$	—	45	65	ns	Figure 4-1, Figure 4-2
Propagation Delay Time	$t_{D2}$	—	45	65	ns	Figure 4-1, Figure 4-2

- Note 1:** Switching times are ensured by design.  
**Note 2:** Tested during characterization, not production tested.

## DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE)<sup>(2)</sup> (CONTINUED)

Electrical Specifications: Unless otherwise indicated, operating temperature range with $4.5V \leq V_{DD} \leq 18V$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Enable Function (ENB_A, ENB_B)</b>						
High-Level Input Voltage	$V_{EN\_H}$	2.4	—	—	V	$V_{DD} = 12V$ , Low-to-High Transition
Low-Level Input Voltage	$V_{EN\_L}$	—	—	0.8	V	$V_{DD} = 12V$ , High-to-Low Transition
Hysteresis	$V_{HYST}$	—	0.4	—	V	
Enable Pull-up Impedance	$R_{ENBL}$	0.7	1.6	3.0	M $\Omega$	$V_{DD} = 14V$ , ENB_A = ENB_B = GND
Propagation Delay Time	$t_{D3}$	—	60	80	ns	Figure 4-3
Propagation Delay Time	$t_{D4}$	—	70	85	ns	Figure 4-3
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	4.5	—	18.0	V	
Supply Current	$I_{DD}$	—	1400	2200	$\mu A$	$V_{IN\_A} = 3V$ , $V_{IN\_B} = 3V$ , ENB_A = ENB_B = High
	$I_{DD}$	—	800	1100	$\mu A$	$V_{IN\_A} = 0V$ , $V_{IN\_B} = 0V$ , ENB_A = ENB_B = High
	$I_{DD}$	—	1300	2000	$\mu A$	$V_{IN\_A} = 3V$ , $V_{IN\_B} = 0V$ , ENB_A = ENB_B = High
	$I_{DD}$	—	1300	2000	$\mu A$	$V_{IN\_A} = 0V$ , $V_{IN\_B} = 3V$ , ENB_A = ENB_B = High
	$I_{DD}$	—	800	1200	$\mu A$	$V_{IN\_A} = 3V$ , $V_{IN\_B} = 3V$ , ENB_A = ENB_B = Low
	$I_{DD}$	—	500	600	$\mu A$	$V_{IN\_A} = 0V$ , $V_{IN\_B} = 0V$ , ENB_A = ENB_B = Low
	$I_{DD}$	—	600	900	$\mu A$	$V_{IN\_A} = 3V$ , $V_{IN\_B} = 0V$ , ENB_A = ENB_B = Low
	$I_{DD}$	—	600	900	$\mu A$	$V_{IN\_A} = 0V$ , $V_{IN\_B} = 3V$ , ENB_A = ENB_B = Low

**Note 1:** Switching times are ensured by design.

**2:** Tested during characterization, not production tested.

## TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+125	$^{\circ}C$	
Maximum Junction Temperature	$T_J$	—	—	+150	$^{\circ}C$	
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}C$	
<b>Package Thermal Resistances</b>						
Thermal Resistance, 8L-6x5 DFN	$\theta_{JA}$	—	35.7	—	$^{\circ}C/W$	Typical four-layer board with vias to ground plane
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	89.3	—	$^{\circ}C/W$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	149.5	—	$^{\circ}C/W$	

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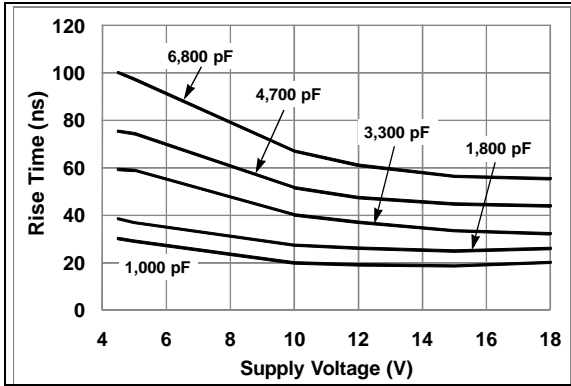
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NOTES:

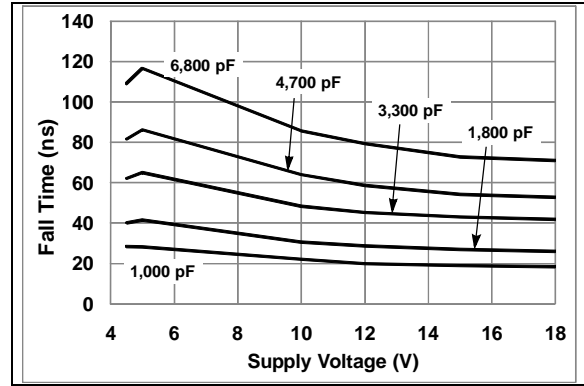
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

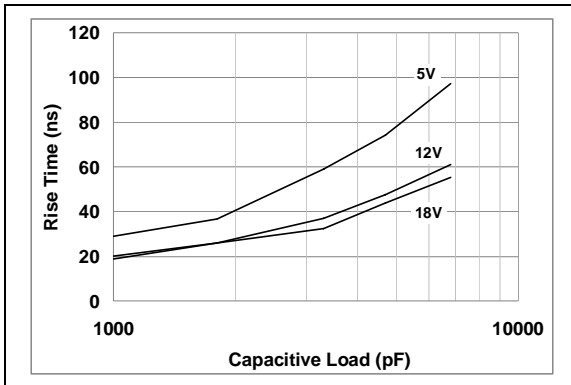
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$  with  $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .



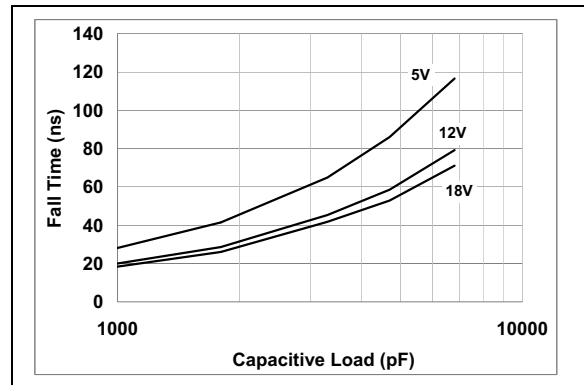
**FIGURE 2-1:** Rise Time vs. Supply Voltage.



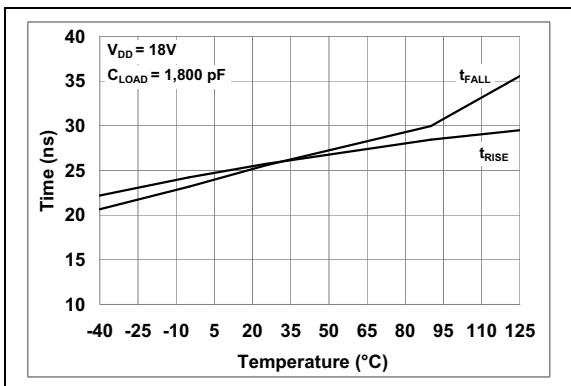
**FIGURE 2-4:** Fall Time vs. Supply Voltage.



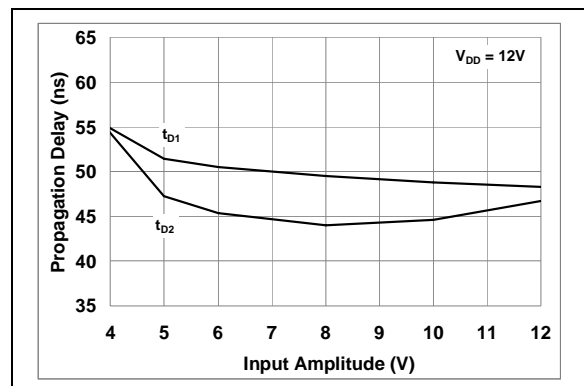
**FIGURE 2-2:** Rise Time vs. Capacitive Load.



**FIGURE 2-5:** Fall Time vs. Capacitive Load.



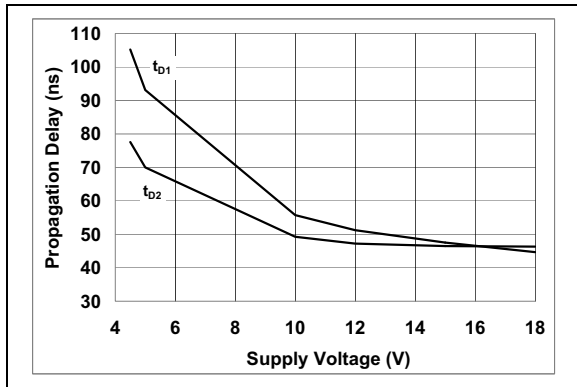
**FIGURE 2-3:** Rise and Fall Times vs. Temperature.



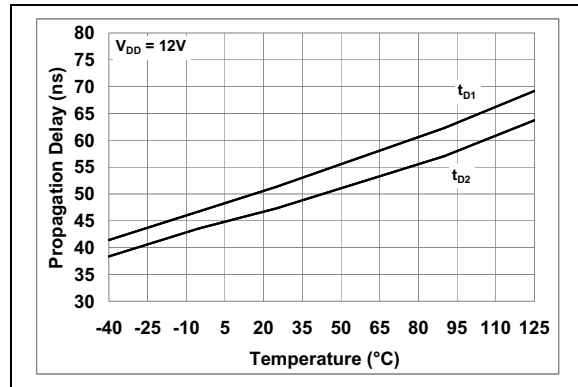
**FIGURE 2-6:** Propagation Delay vs. Input Amplitude.

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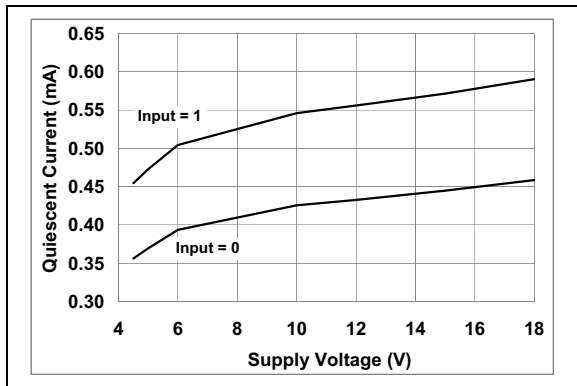
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$  with  $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .



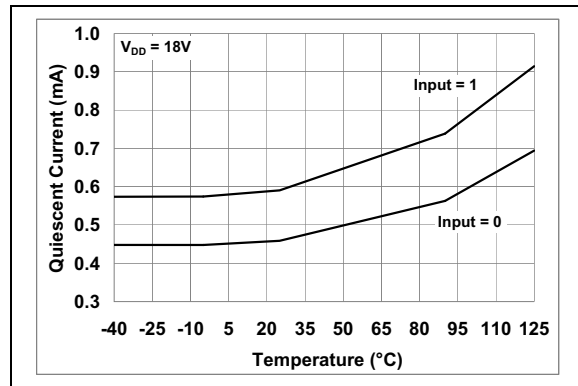
**FIGURE 2-7:** Propagation Delay Time vs. Supply Voltage.



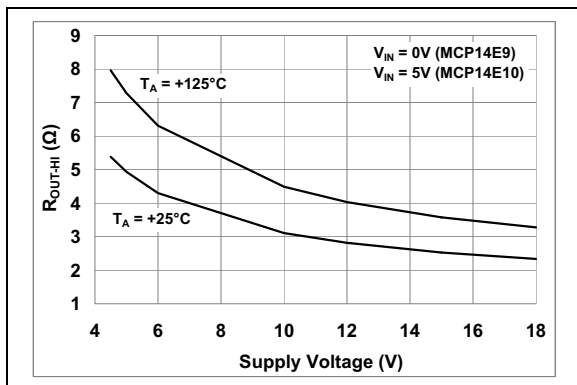
**FIGURE 2-10:** Propagation Delay Time vs. Temperature.



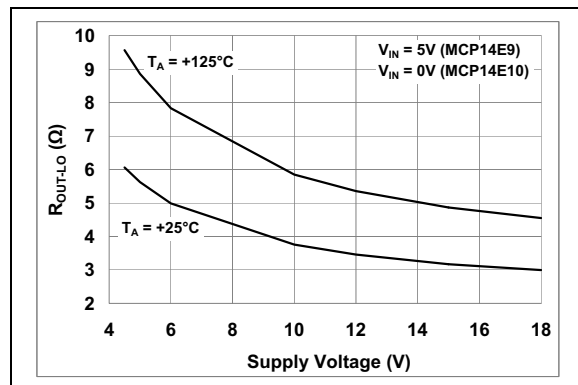
**FIGURE 2-8:** Quiescent Current vs. Supply Voltage.



**FIGURE 2-11:** Quiescent Current vs. Temperature.



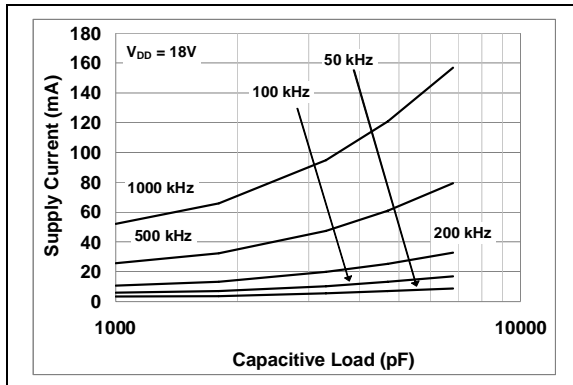
**FIGURE 2-9:** Output Resistance (Output High) vs. Supply Voltage.



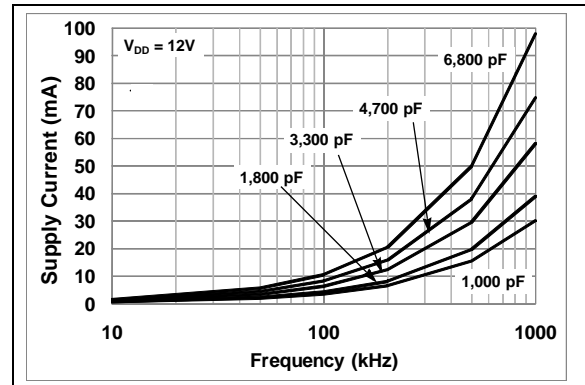
**FIGURE 2-12:** Output Resistance (Output Low) vs. Supply Voltage.



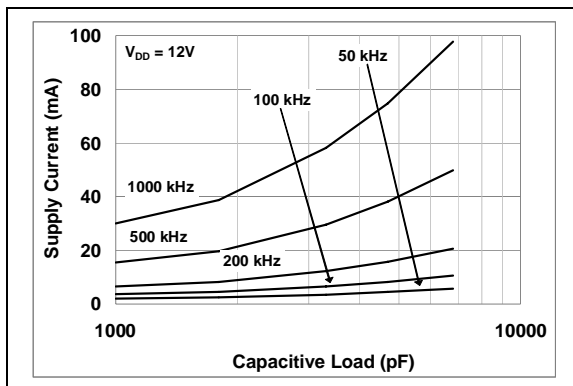
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$  with  $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .



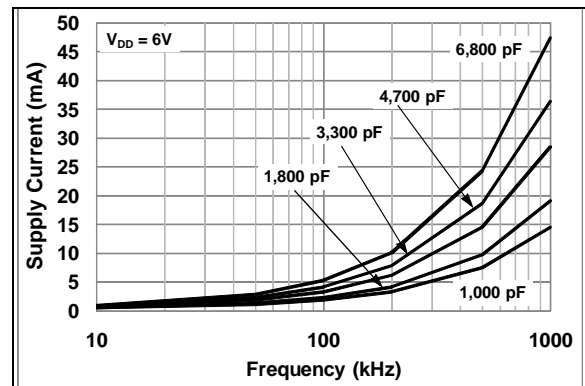
**FIGURE 2-13:** Supply Current vs. Capacitive Load.



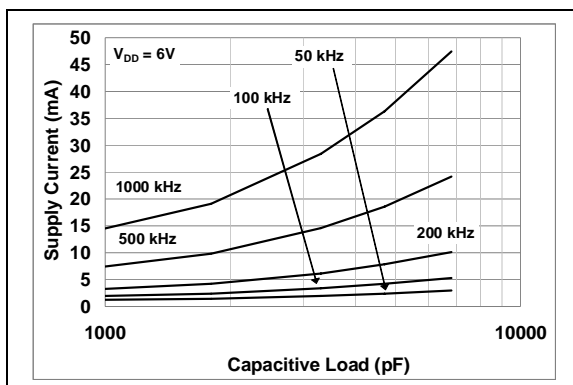
**FIGURE 2-16:** Supply Current vs. Frequency.



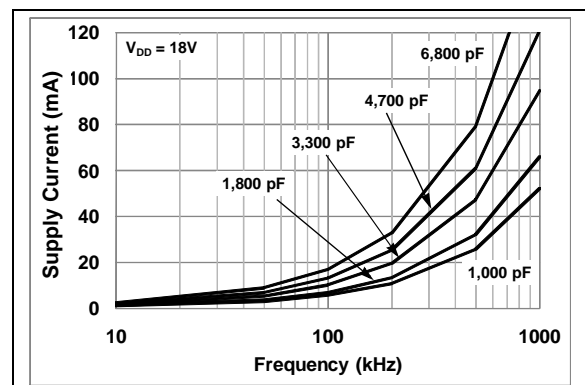
**FIGURE 2-14:** Supply Current vs. Capacitive Load.



**FIGURE 2-17:** Supply Current vs. Frequency.



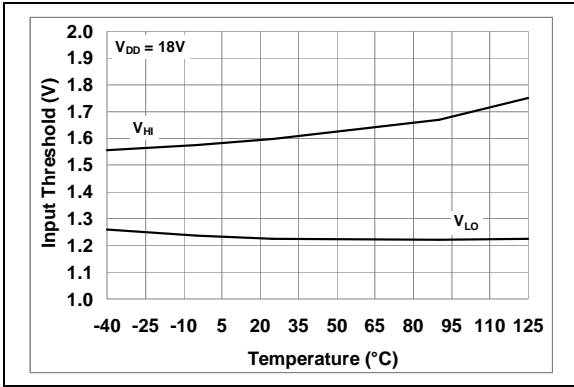
**FIGURE 2-15:** Supply Current vs. Capacitive Load.



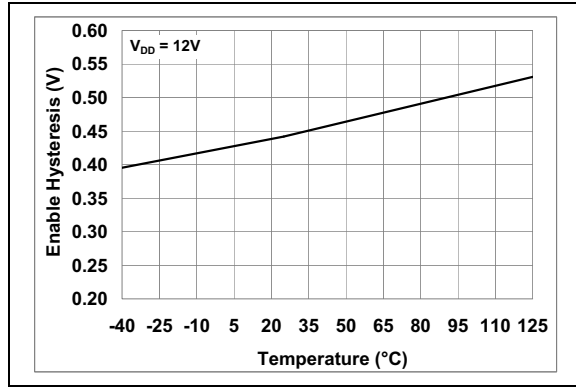
**FIGURE 2-18:** Supply Current vs. Frequency.

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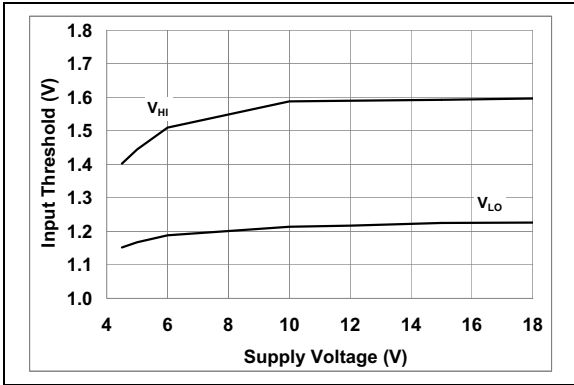
Note: Unless otherwise indicated,  $T_A = +25^\circ\text{C}$  with  $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ .



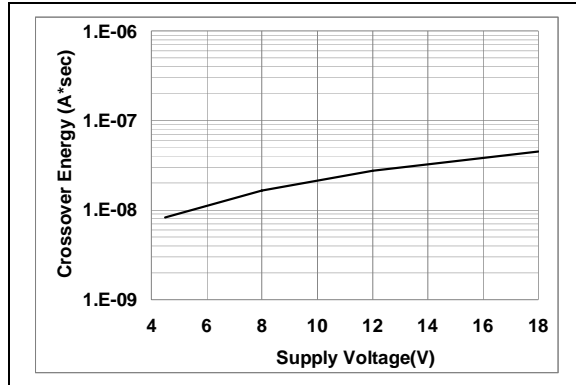
**FIGURE 2-19:** Input Threshold vs. Temperature.



**FIGURE 2-22:** Enable Hysteresis vs. Temperature.

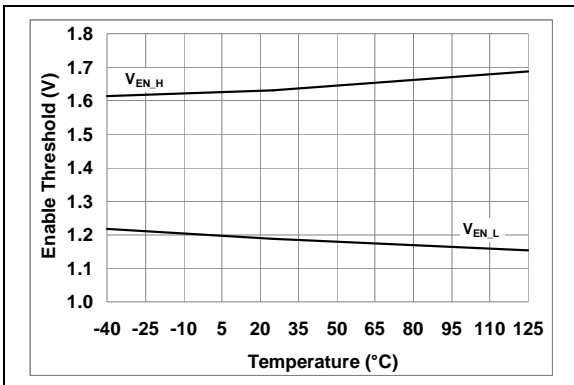


**FIGURE 2-20:** Input Threshold vs. Supply Voltage.



**Note:** The values in this graph represent the loss seen by both drivers in a package during a complete cycle.  
For a single driver, divide the stated value by 2.  
For a single transition of a single driver, divide the stated value by 4.

**FIGURE 2-23:** Crossover Energy vs. Supply Voltage.



**FIGURE 2-21:** Enable Threshold vs. Temperature.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

PDIP, SOIC, 6x5 DFN	Symbol			Description
	MCP14E9	MCP14E10	MCP14E11	
1	ENB_A	ENB_A	ENB_A	Output A Enable
2	IN A	IN A	IN A	Input A
3	GND	GND	GND	Ground
4	IN B	IN B	IN B	Input B
5	$\overline{\text{OUT B}}$	OUT B	OUT B	Output B
6	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	Supply Input
7	$\overline{\text{OUT A}}$	OUT A	$\overline{\text{OUT A}}$	Output A
8	ENB_B	ENB_B	ENB_B	Output B Enable
9	EP	EP	EP	Exposed metal pad (DFN package only). Exposed pad is electrically isolated.

### 3.1 Enable A (ENB\_A)

The ENB\_A pin is the enable control for Output A. This enable pin is internally pulled up to V<sub>DD</sub> for active-high operation and can be left floating for standard operation. When the ENB\_A pin is pulled below the enable pin, Low Level Input Voltage (V<sub>EN\_L</sub>), Output A will be in the OFF state, regardless of the input pin state.

### 3.2 Control Inputs A and B (IN A; IN B)

The MOSFET driver inputs are a high-impedance TTL/CMOS compatible input. The inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

### 3.3 Ground (GND)

Ground is the device return pin. The ground pin should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin when the capacitive load is being discharged.

### 3.4 Outputs A and B (OUT A; OUT B)

Outputs, A and B, are CMOS push-pull outputs that are capable of sourcing and sinking 3.0A of peak current (V<sub>DD</sub> = 18V). The low output impedance ensures the gate of the MOSFET will stay in the intended state, even during large transients.

### 3.5 Supply Input (V<sub>DD</sub>)

V<sub>DD</sub> is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

### 3.6 Enable B (ENB\_B)

The ENB\_B pin is the enable control for Output B. This enable pin is internally pulled up to V<sub>DD</sub> for active-high operation, and can be left floating for standard operation. When the ENB\_B pin is pulled below the enable pin, Low-Level Input Voltage (V<sub>EN\_L</sub>), Output B will be in the OFF state, regardless of the input pin state.

### 3.7 Exposed Metal Pad (EP)

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane, or other copper plane on a printed circuit board, to aid in heat removal from the package.

# MCP14E9/10/11

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NOTES:

## 4.0 APPLICATION INFORMATION

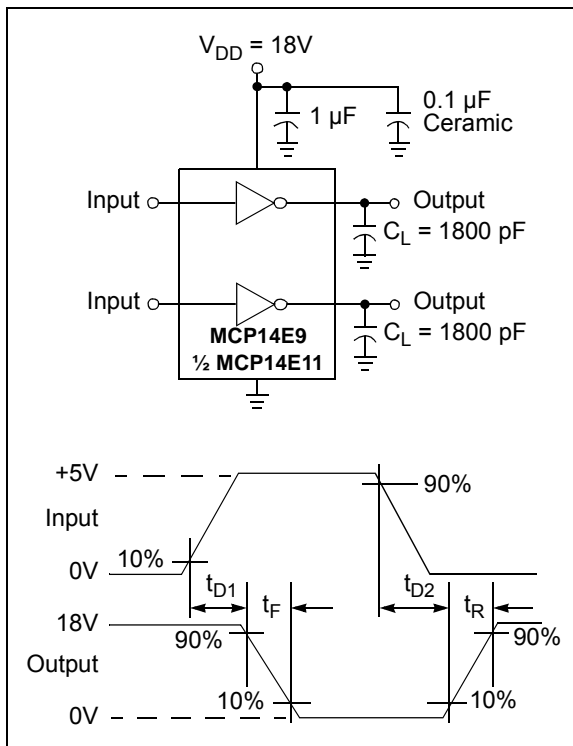
### 4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high-peak currents to charge/discharge the gate capacitance of external MOSFETs, or insulated gate bipolar transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. MOSFET drivers, like the MCP14E9/10/11 family, can be used to provide additional source/sink current capability.

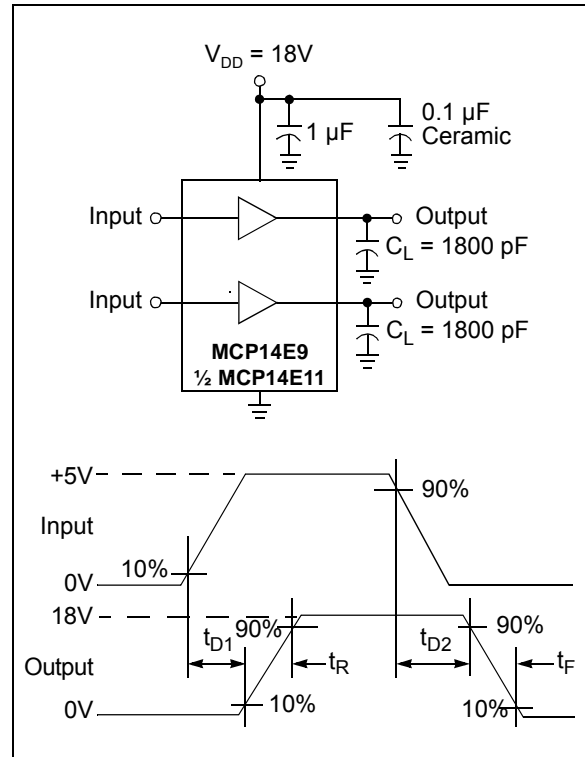
An additional degree of control has been added to the MCP14E9/10/11 family. There are separate enable functions for each driver that allow for the immediate termination of the output pulse, regardless of the state of the input signal.

### 4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully OFF state to a fully ON state are characterized by the drivers' rise time ( $t_R$ ), fall time ( $t_F$ ) and propagation delays ( $t_{D1}$  and  $t_{D2}$ ). The MCP14E9/10/11 family of drivers can typically charge and discharge an 1800 pF load capacitance in approximately 15 ns, along with a typical matched propagation delay of 45 ns. [Figure 4-1](#) and [Figure 4-2](#) show the test circuit and timing waveform used to verify the MCP14E9/10/11 timing.



**FIGURE 4-1:** Inverting Driver Timing Waveform.



**FIGURE 4-2:** Non-Inverting Driver Timing Waveform.

### 4.3 Enable Function

The ENB\_A and ENB\_B enable pins allow the independent control of OUT A and OUT B, respectively. They are active-high and are internally pulled up to  $V_{DD}$ , so that the default state is to enable the driver. These pins can be left floating for normal operation.

When an enable pin voltage is above the enable pin high threshold voltage,  $V_{EN\_H}$ , that driver output is enabled and allowed to react to changes in the INPUT pin voltage state. Similarly, when the enable pin voltage falls below the enable pin low threshold voltage,  $V_{EN\_L}$ , that driver output is disabled and does not respond to the changes in the INPUT pin voltage state. When the driver is disabled, the output goes to a low state. Refer to [Table 4-1](#) for enable pin logic. The threshold voltages of the enable function are compatible with logic levels. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching. For robust designs, it is recommended that the slew rate of the enable pin signal be greater than 1V/ns.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays,  $t_{D3}$  and  $t_{D4}$ , are graphically represented in [Figure 4-3](#).

# MCP14E9/10/11

TABLE 4-1: ENABLE PIN LOGIC

ENB_A	ENB_B	IN A	IN B	MCP14E9		MCP14E10		MCP14E11	
				OUT A	OUT B	OUT A	OUT B	OUT A	OUT B
H	H	H	H	L	L	H	H	L	H
H	H	H	L	L	H	H	L	L	L
H	H	L	H	H	L	L	H	H	H
H	H	L	L	H	H	L	L	H	L
L	L	X	X	L	L	L	L	L	L

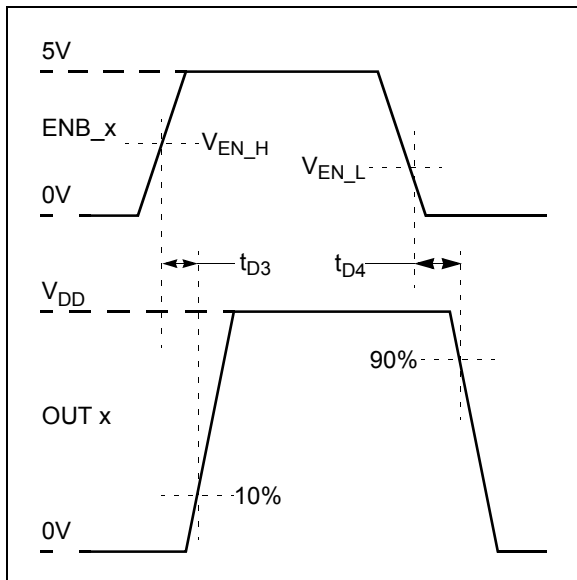


FIGURE 4-3: Enable Timing Waveform.

## 4.4 Decoupling Capacitors

Careful layout and decoupling capacitors are highly recommended when using MOSFET drivers. Large currents are required to charge and discharge capacitive loads quickly. For example, approximately 2.0A are needed to charge an 1800 pF load with 18V in 15 ns.

To operate the MOSFET driver over a wide frequency range, with low supply impedance, a ceramic and low-ESR film capacitors are recommended to be placed in parallel, between the driver,  $V_{DD}$  and GND. A 1.0  $\mu$ F, low-ESR film capacitor and a 0.1  $\mu$ F ceramic capacitor placed between pins, 6 and 3, should be used. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

## 4.5 PCB Layout Considerations

A proper PCB layout is important in a high-current, fast switching circuit, to provide proper device operation and robustness to the design. The PCB trace loop area and inductance should be minimized by the use of ground planes or trace under MOSFET gate drive signals, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP14E9/10/11 will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

## 4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements (Equation 4-1).

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

- $P_T$  = Total Power Dissipation
- $P_L$  = Load Power Dissipation
- $P_Q$  = Quiescent Power Dissipation
- $P_{CC}$  = Operating Power Dissipation

### 4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is:

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

- $f$  = Switching Frequency
- $C_T$  = Total Load Capacitance
- $V_{DD}$  = MOSFET Driver Supply Voltage

## 4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends upon the state of the input pin. The MCP14E9/10/11 devices have a quiescent current draw with a Logic '1' on the input pin of 1 mA (typical) and 300  $\mu$ A (typical) with a Logic '0'. The quiescent power dissipation is:

### EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

$I_{QH}$  = Quiescent current in the high state

$D$  = Duty cycle

$I_{QL}$  = Quiescent current in the low state

$V_{DD}$  = MOSFET driver supply voltage

## 4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions, because for a very short period of time, both MOSFETs in the output stage are ON, simultaneously. This cross-conduction current leads to a power dissipation described as:

### EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

Where:

$CC$  = Cross-Conduction Constant (A \* sec)

$f$  = Switching Frequency

$V_{DD}$  = MOSFET Driver Supply Voltage

# MCP14E9/10/11

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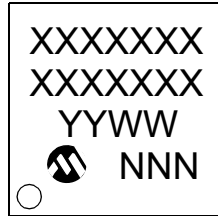
NOTES:



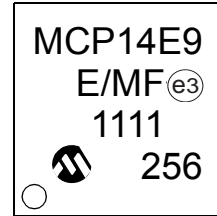
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

8-Lead DFN-S (5x6x1 mm)



Example



8-Lead PDIP



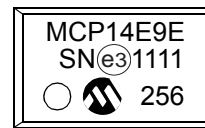
Example



8-Lead SOIC (.150")



Example

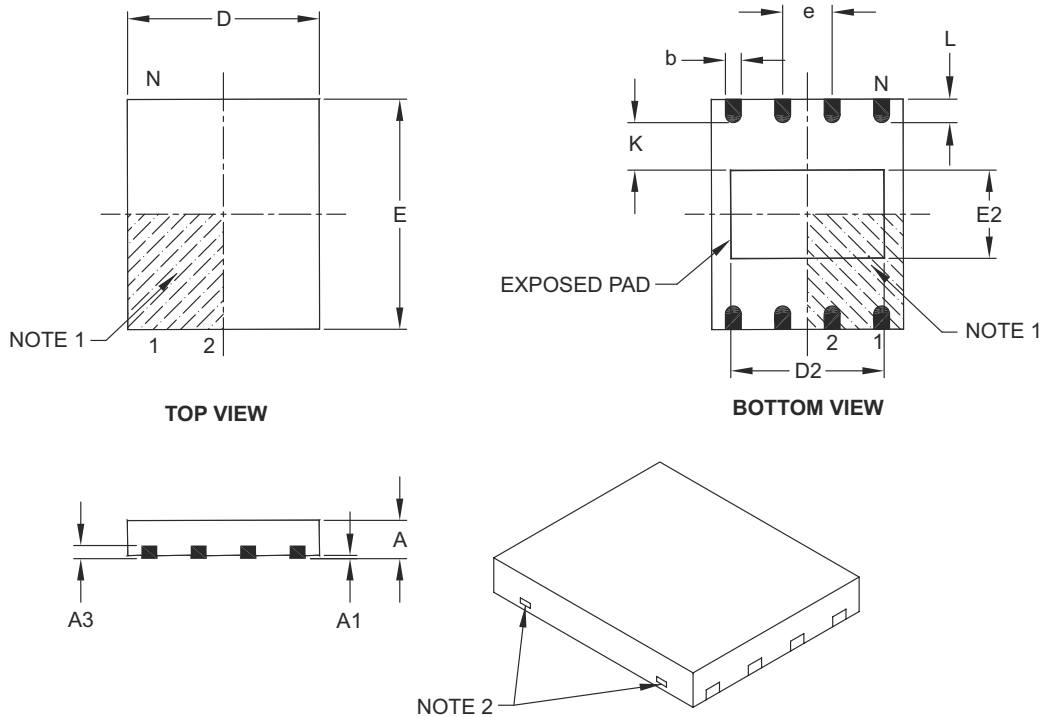


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

# MCP14E9/10/11

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Overall Width	E	6.00 BSC		
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

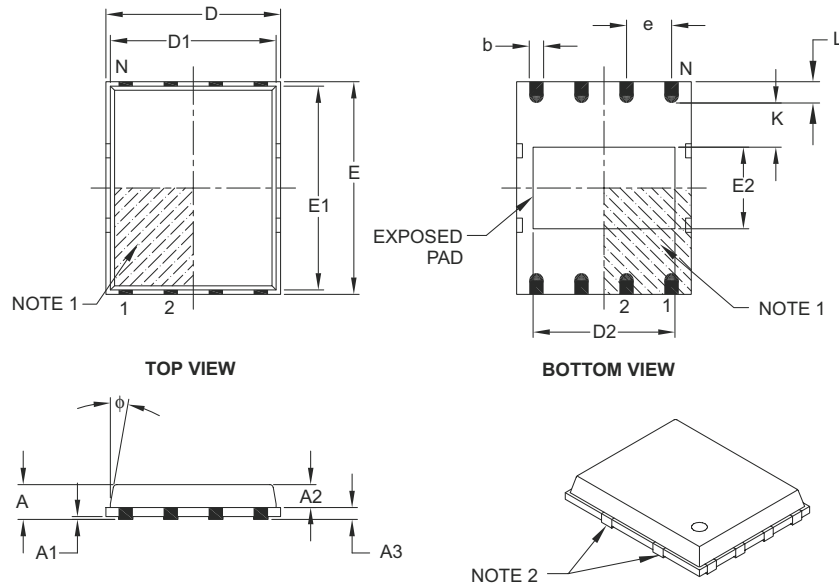
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A	–	0.85	1.00	
Molded Package Thickness	A2	–	0.65	0.80	
Standoff	A1	0.00	0.01	0.05	
Base Thickness	A3		0.20 REF		
Overall Length	D		4.92 BSC		
Molded Package Length	D1		4.67 BSC		
Exposed Pad Length	D2	3.85	4.00	4.15	
Overall Width	E		5.99 BSC		
Molded Package Width	E1		5.74 BSC		
Exposed Pad Width	E2	2.16	2.31	2.46	
Contact Width	b	0.35	0.40	0.47	
Contact Length	L	0.50	0.60	0.75	
Contact-to-Exposed Pad	K	0.20	–	–	
Model Draft Angle Top	$\phi$	–	–	12°	

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

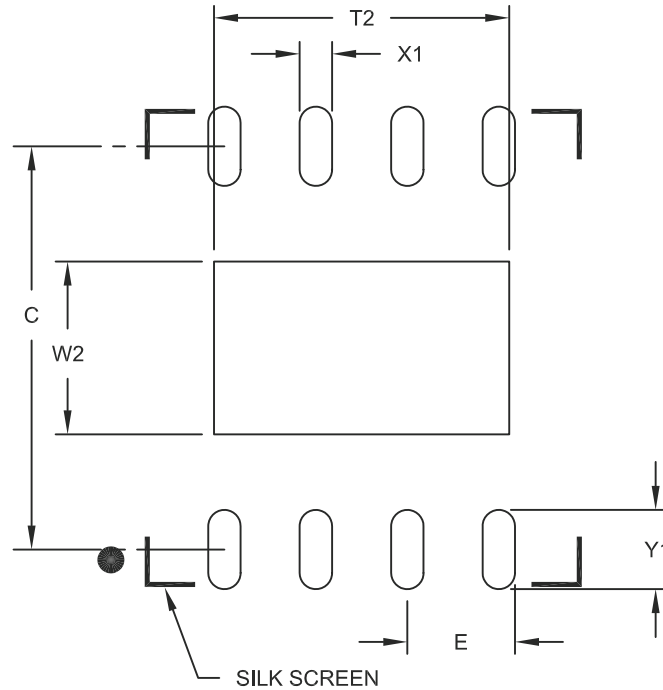
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

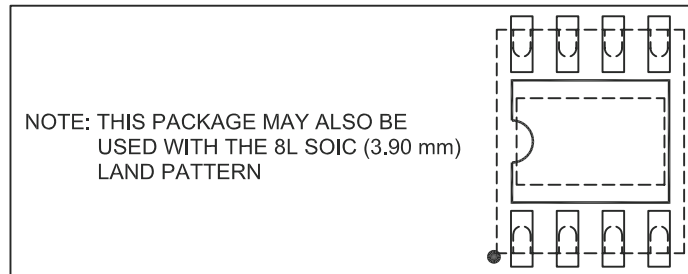
# MCP14E9/10/11

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

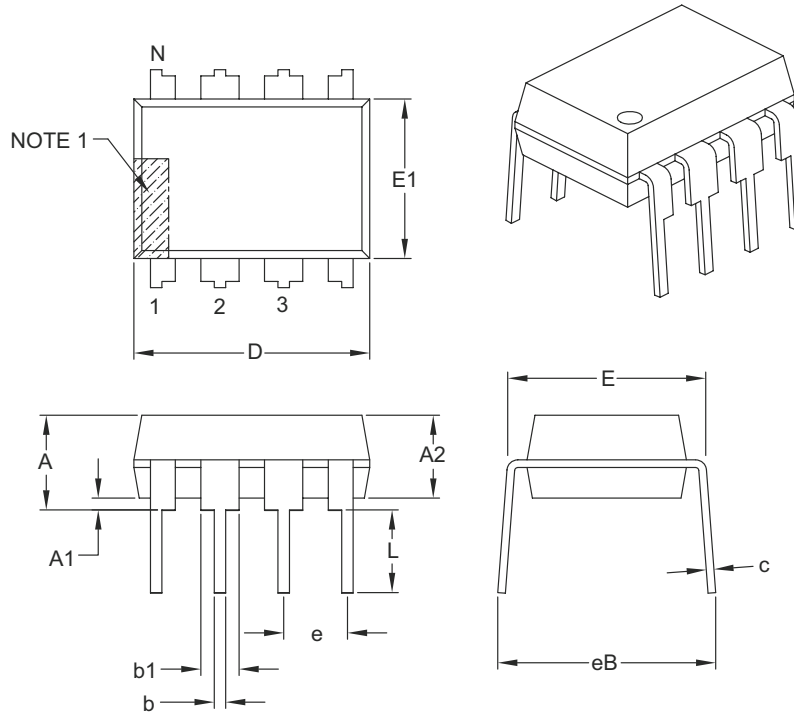
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

**Notes:**

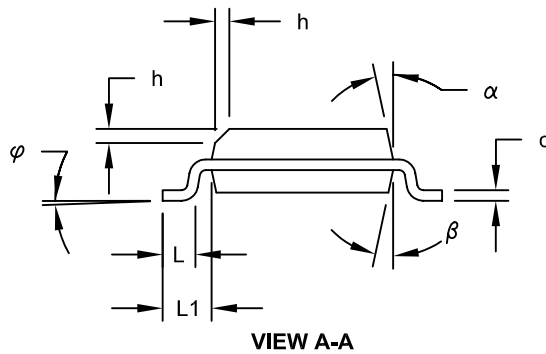
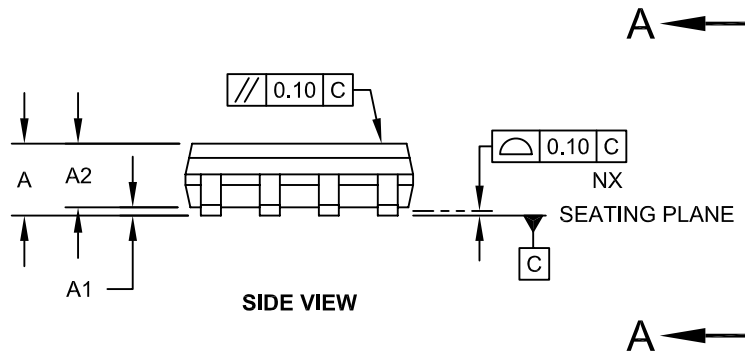
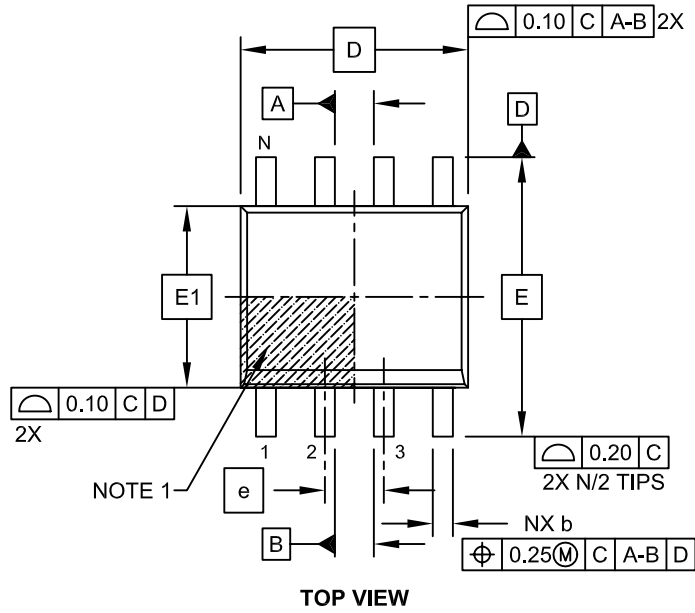
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

# MCP14E9/10/11

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

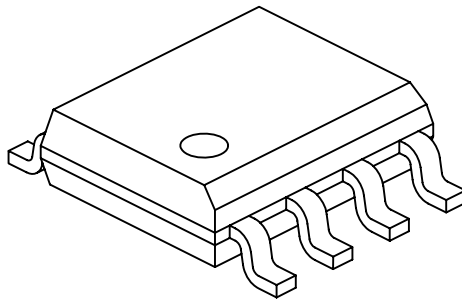
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

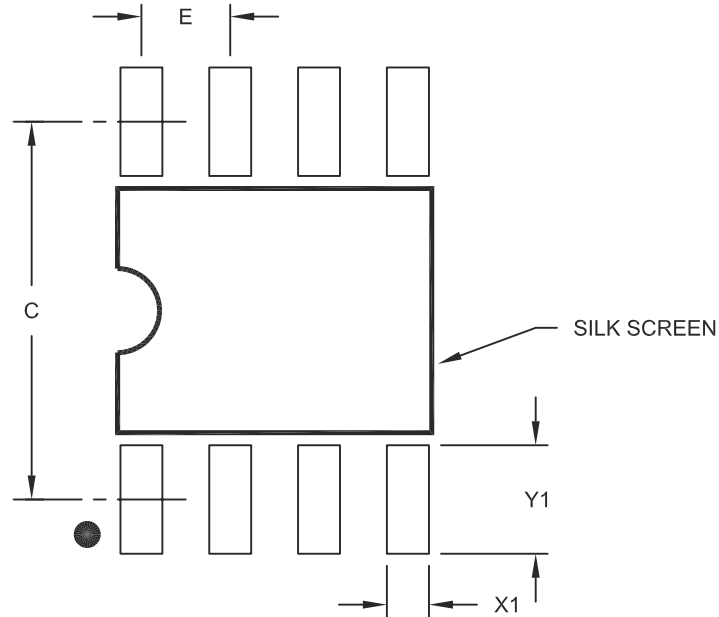
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

# MCP14E9/10/11

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A



## APPENDIX A: REVISION HISTORY

### Revision A (March 2011)

- Original Release of this Document.

# MCP14E9/10/11

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>/XX</u>	
Device	Temperature Range	Package	
Device:	MCP14E9:	3.0A Dual MOSFET Driver, Inverting	
	MCP14E9T:	3.0A Dual MOSFET Driver, Inverting, Tape and Reel (DFN and SOIC only)	
	MCP14E10:	3.0A Dual MOSFET Driver, Non-Inverting	
	MCP14E10T:	3.0A Dual MOSFET Driver, Non-Inverting, Tape and Reel (DFN and SOIC only)	
	MCP14E11:	3.0A Dual MOSFET Driver, Complementary	
	MCP14E11T:	3.0A Dual MOSFET Driver, Complementary, Tape and Reel (DFN and SOIC only)	
Temperature Range:	E	=	-40°C to +125°C
Package: *	MF	=	Dual, Flat, No Lead (6x5 mm Body), 8-lead
	P	=	Plastic DIP, (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
<b>Examples:</b>			
a)	MCP14E9-E/MF:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package.	
b)	MCP14E9T-E/MF:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, Tape and Reel, 8LD 6x5 DFN package.	
c)	MCP14E9-E/P:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package.	
d)	MCP14E9-E/SN:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package.	
e)	MCP14E9T-E/SN:	3.0A Dual Inverting MOSFET Driver, Tape and Reel, Extended Temperature, 8LD SOIC package.	
a)	MCP14E10-E/MF:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package.	
b)	MCP14E10-E/P:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package.	
c)	MCP14E10-E/SN:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package.	
a)	MCP14E11-E/MF:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD 6x5 DFN package.	
b)	MCP14E11-E/P:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD PDIP package.	
c)	MCP14E11-E/SN:	3.0A Dual Inverting MOSFET Driver, Extended Temperature, 8LD SOIC package.	

# MCP14E9/10/11

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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