CA3162, CA3162A

August 1997

A/D Converters for 3-Digit Display

Features

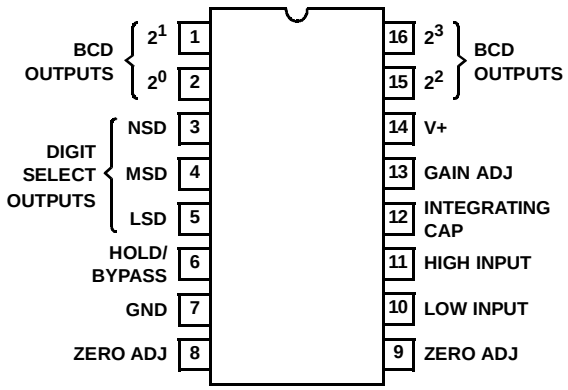
- Dual Slope A/D Conversion
- Multiplexed BCD Display
- Ultra Stable Internal Band Gap Voltage Reference
- Capable of Reading 99mV Below Ground with Single Supply
- Differential Input
- Internal Timing - No External Clock Required
- Choice of Low Speed (4Hz) or High Speed (96Hz) Conversion Rate
- "Hold" Inhibits Conversion but Maintains Delay
- Overrange Indication
  - "EEE" for Reading Greater than +999mV, "-" for Reading More Negative than -99mV When Used With CA3161E
- Extended Temperature Range Version Available

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3162E	0 to 70	16 Ld PDIP	E16.3
CA3162AE	-40 to 85	16 Ld PDIP	E16.3

Pinout

CA3162
(PDIP)
TOP VIEW



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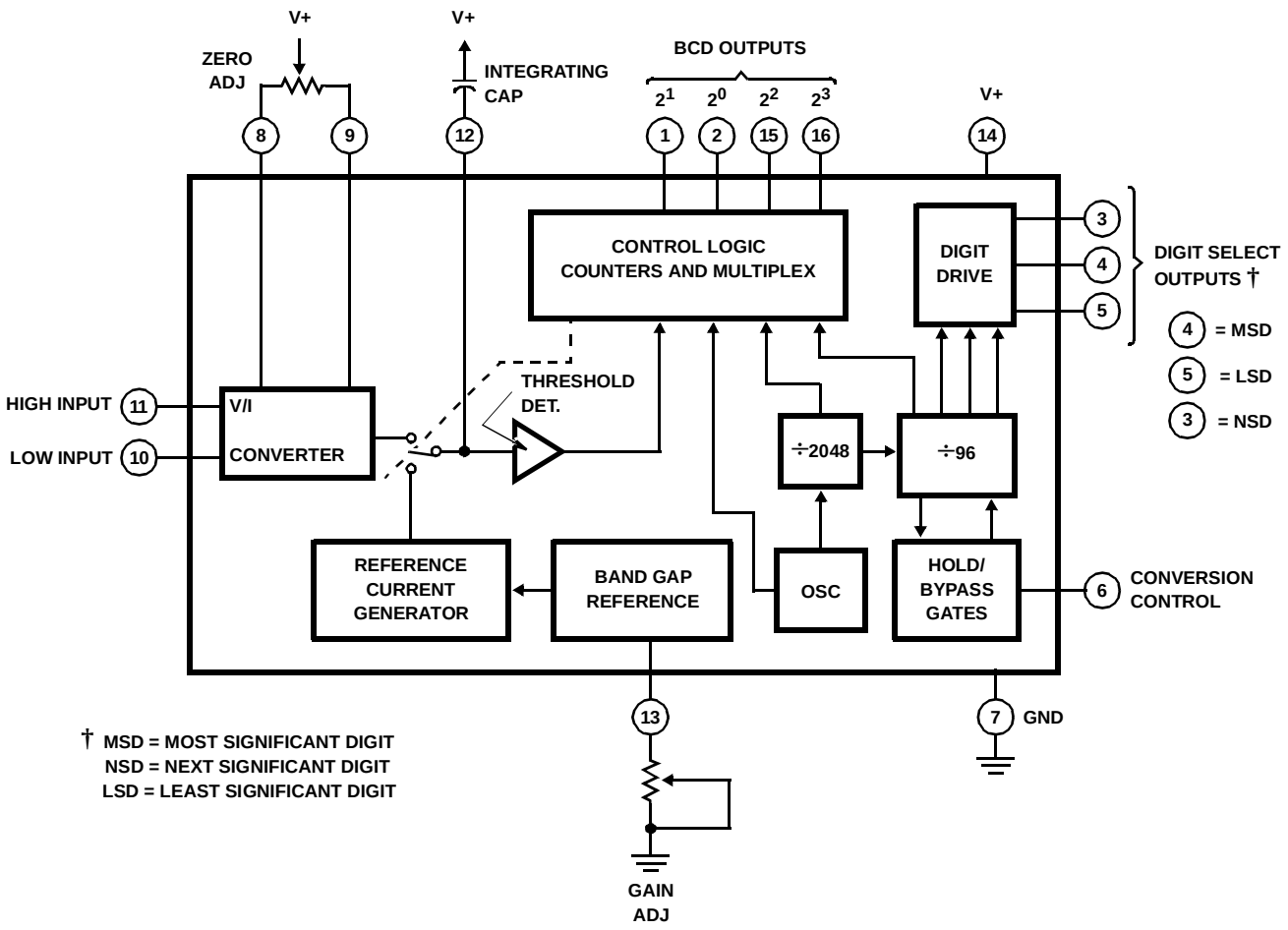
Functional Block Diagram



Absolute Maximum Ratings

DC Supply Voltage (Between Pins 7 and 14) . . . . . +7V
Input Voltage (Pin 10 or 11 to Ground) . . . . . ±15V

Operating Conditions

Temperature Range
CA3162E . . . . . 0 to 75^{o}C
CA3162AE . . . . . -40^{o}C to 85^{o}C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP Package	90

Maximum Junction Temperature . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25^{o}C, V+ = 5V, Zero Pot Centered, Gain Pot = 2.4kΩ, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range, V+		4.5	5	5.5	V
Supply Current, I+	100kΩ to V+ on Pins 3, 4, 5	-	-	17	mA
Input Impedance, Z_I		-	100	-	MΩ
Input Bias Current, I_{IB}	Pins 10 and 11	-	-80	-	nA
Unadjusted Zero Offset	V_{11}-V_{10} = 0V, Read Decoded Output	-12	-	+12	mV
Unadjusted Gain	V_{11}-V_{10} = 900mV, Read Decoded Output	846	-	954	mV
Linearity	Notes 1 and 2	-1	-	+1	Count
Conversion Rate					
Slow Mode	Pin 6 = Open or GND	-	4	-	Hz
Fast Mode	Pin 6 = 5V	-	96	-	Hz
Conversion Control Voltage (Hold Mode) at Pin 6		0.8	1.2	1.6	V
Common Mode Input Voltage Range, V_{ICR}	Notes 3, 4	-0.2	-	+0.2	V
BCD Sink Current at Pins 1, 2, 15, 16	$V_{BCD} \geq$ 0.5V, at Logic Zero State	0.4	1.6	-	mA
Digit Select Sink Current at Pins 3, 4, 5	V_{DIGIT} Select = 4V at Logic Zero State	1.6	2.5	-	mA
Zero Temperature Coefficient	V_I = 0V, Zero Pot Centered	-	10	-	μV/^{o}V
Gain Temperature Coefficient	V_I = 900mV, Gain Pot = 2.4kΩ	-	0.005	-	%/^{o}C

NOTES:

1. Apply 0V across V_{11} to V_{10}. Adjust zero potentiometer to give 000mV reading. Apply 900mV to input and adjust gain potentiometer to give 900mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ±0.5 count bit digitizing error.
3. For applications where low input pin 10 is not operated at pin 7 potential, a return path of not more than 100kΩ resistance must be provided for input bias currents.
4. The common mode input voltage above ground cannot exceed +0.2V if the full input signal range of 999mV is required at pin 11. That is, pin 11 may not operate higher than 1.2V positive with respect to ground or 0.2V negative with respect to ground. If the maximum input signal is less than 999mV, the common mode input voltage may be raised accordingly.

Timing Diagram

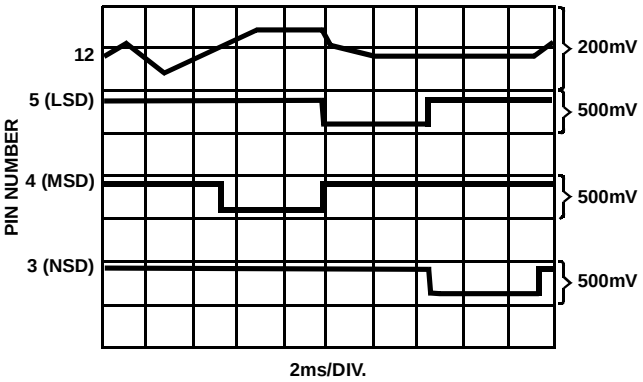


FIGURE 1. HIGH SPEED MODE

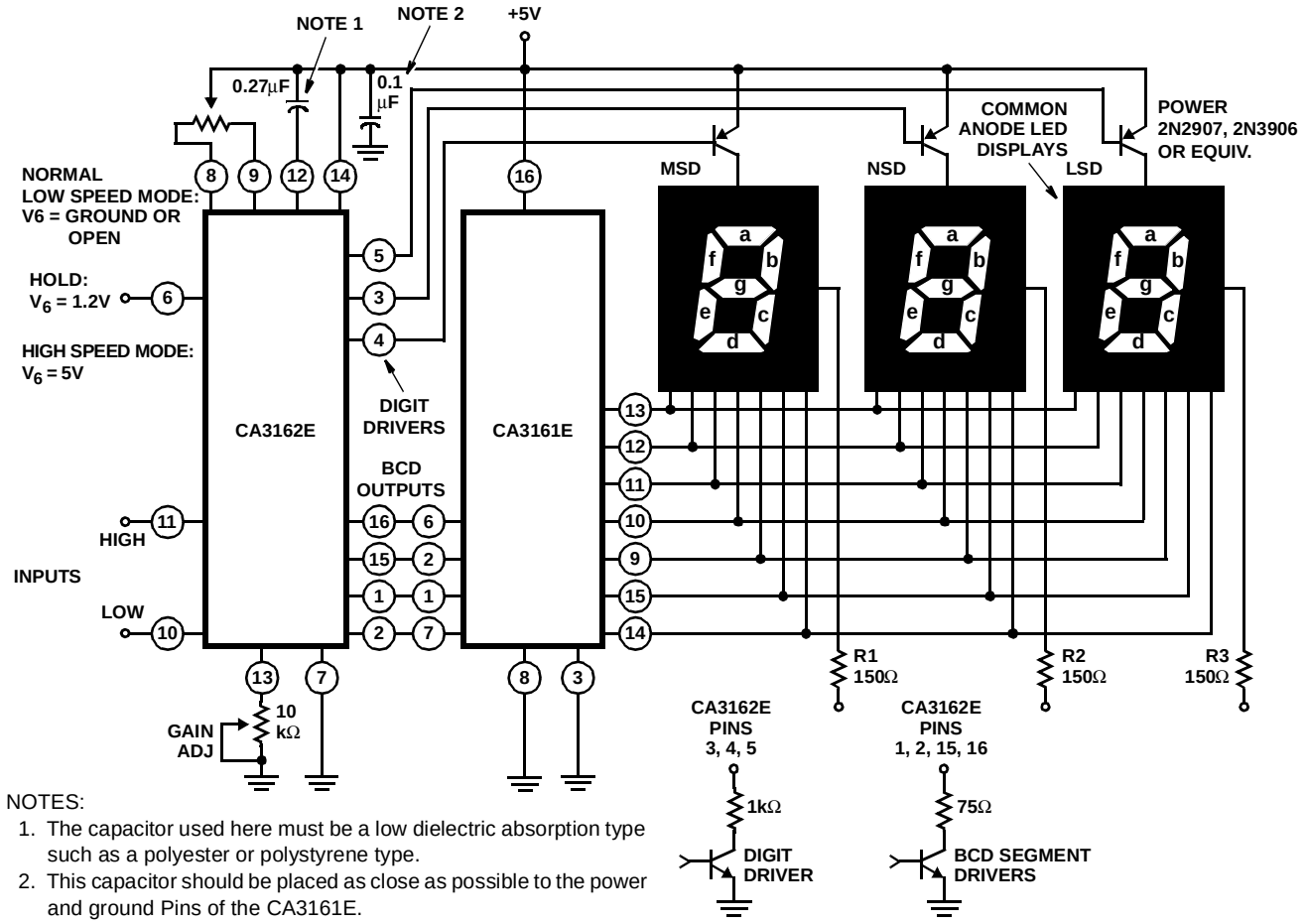
Detailed Description

The Functional Block Diagram of the CA3162E shows the V/I converter and reference current generator, which is the heart of the system. The V/I converter converts the input voltage applied between pins 10 and 11 to a current that charges the integrating capacitor on pin 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band gap reference constant current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786Hz ring oscillator, and the input at pin 6 determines the sampling rate. A 5V input provides a high speed sampling rate (96Hz), and grounding or floating pin 6 provides a low speed (4Hz) sampling rate. When pin 6 is fixed at +1.2V (by placing a 12K resistor between pin 6 and the +5V supply) a “hold” feature is available. While the CA3162E is in the hold mode, sampling continues at 4Hz but the display data are latched to the last reading prior to the application of the 1.2V. Removal of the 1.2V restores continuous display changes. Note, however, that the sampling rate remains at 4Hz.

Figure 1 shows the timing of sampling and digit select pulses for the high speed mode. Note that the basic A/D conversion process requires approximately 5ms in both modes.

The “EEE” or “---” displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to -99mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).



NOTES:

1. The capacitor used here must be a low dielectric absorption type such as a polyester or polystyrene type.
2. This capacitor should be placed as close as possible to the power and ground Pins of the CA3161E.

FIGURE 2. BASIC DIGITAL READOUT SYSTEM USING THE CA3162E AND THE CA3161E

CA3162E Liquid Crystal Display (LCD) Application

Figure 3 shows the CA3162E in a typical LCD application. LCDs may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCDs must be driven by an AC signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

The capacitors on the outputs of inverters G3 and G4 filter out the decode spikes on the MSD and NSD signals. The capacitors and pull-up resistors connected to the MSD, NSD and LSD outputs are there to shorten the digit drive signal thereby providing proper timing for the CD4056B latches.

Inverters G1 and G2 are used as an astable multivibrator to provide the AC drive to the LCD backplane. Inverters G3, G4 and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to CMOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (-) as an “L” and the positive overload indicator (E) as an “H”.

The circuit as shown in Figure 3 using G7, G8 and G9 will decode the negative sign (-) as a negative sign (-), and the positive overload indicator (E) as “H”.

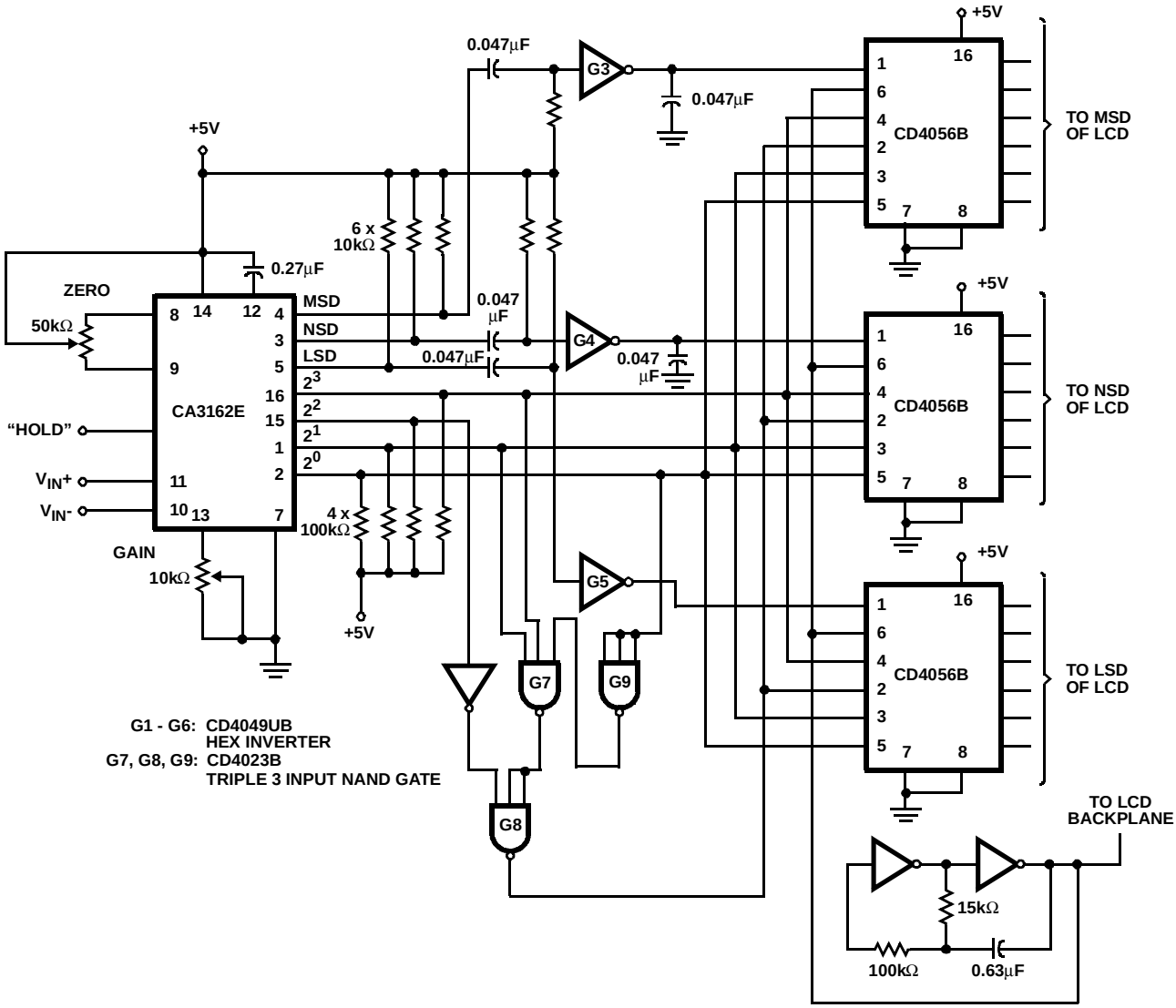


FIGURE 3. TYPICAL LCD APPLICATION

CA3162E Common-Cathode, LED Display Application

Figure 4 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank, instead of (-), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Figure 4 restores the negative sign (-), allowing the display of negative numbers as low as -99mV. Negative overrange is indicated by a negative sign (-) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed.

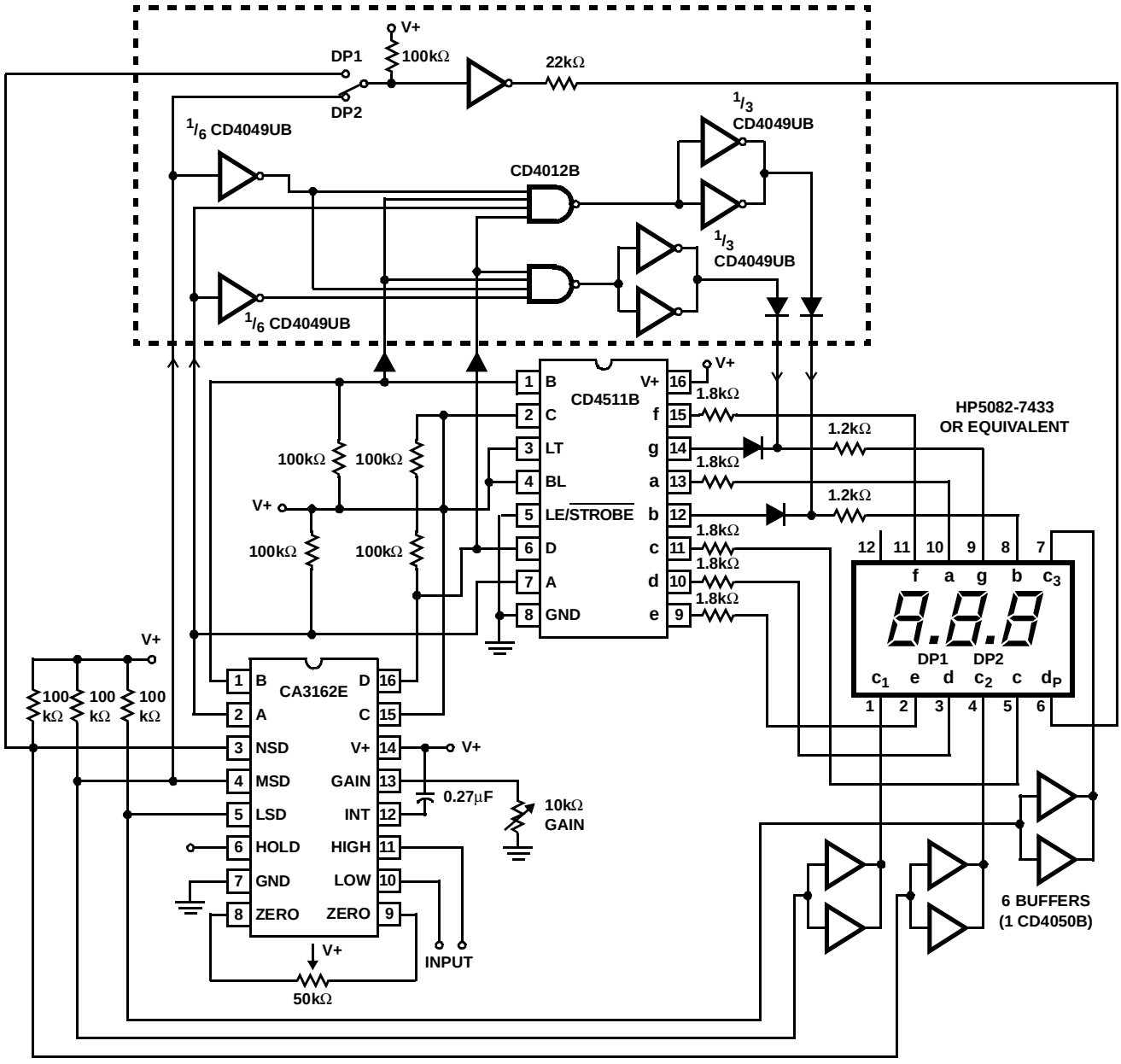


FIGURE 4. TYPICAL COMMON-CATHODE LED APPLICATION

Die Characteristics

DIE DIMENSIONS:

101 mils x 124 mils x 20 mils ±1 mil

METALLIZATION:

Type: Al
Thickness: 17.5kÅ ±2.5kÅ

PASSIVATION:

Type: 3% PSG
Thickness: 13kÅ ±2.5kÅ

Metallization Mask Layout

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